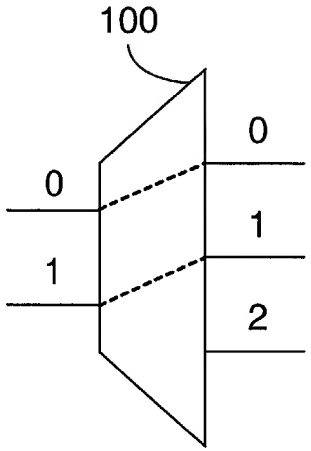



FIG. 1A

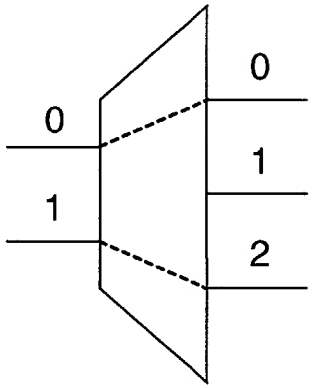



FIG. 1B

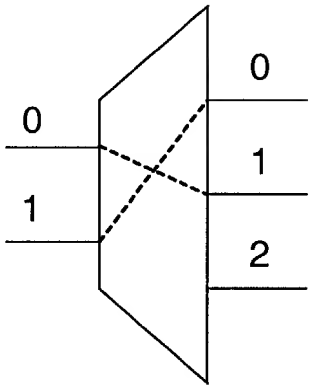



FIG. 1C

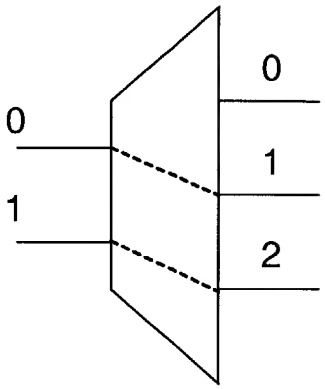



FIG. 1D

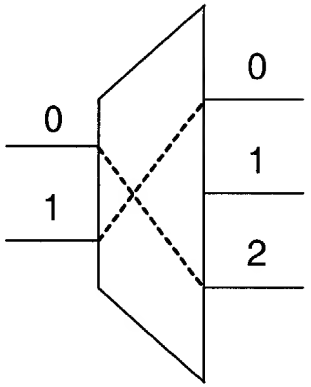



FIG. 1E

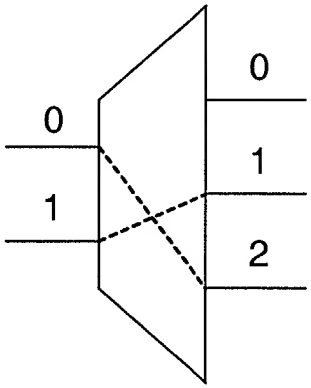



FIG. 1F

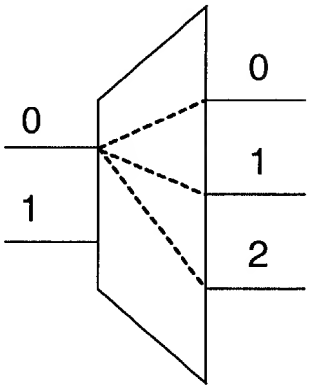



FIG. 1G

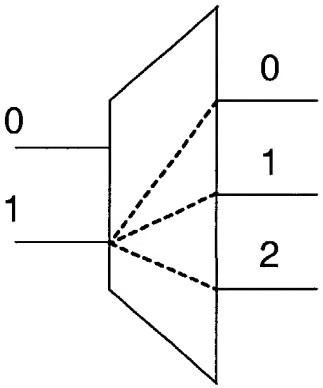



FIG. 1H

Test Station

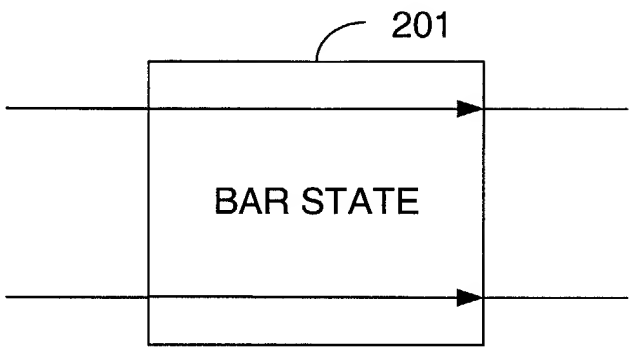



FIG. 2A

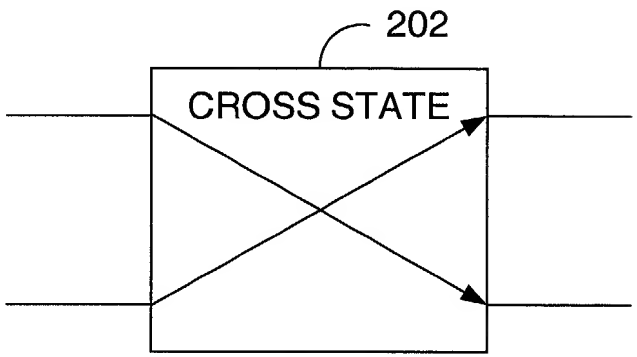



FIG. 2B

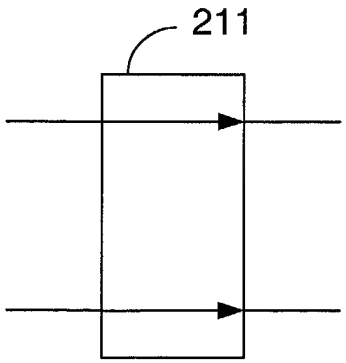



FIG. 2C

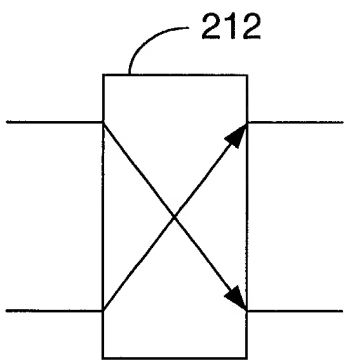



FIG. 2D

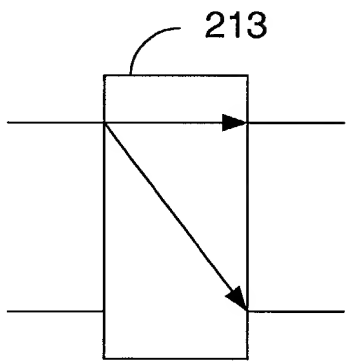



FIG. 2E

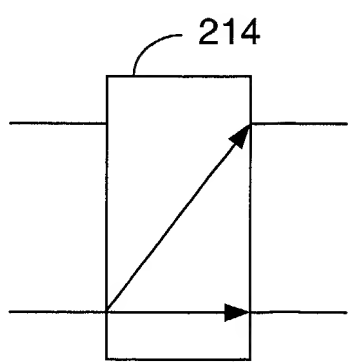



FIG. 2F

POSTSUBMITTED

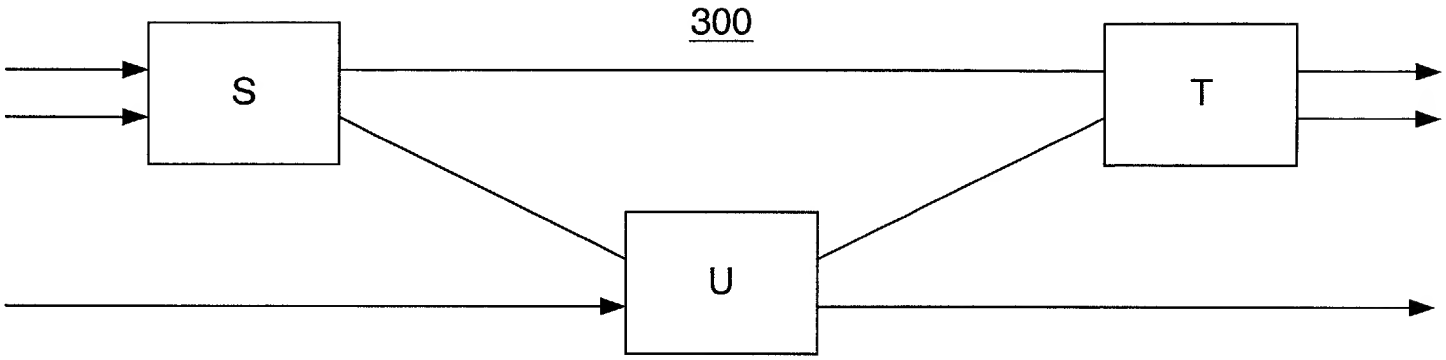



FIG. 3A

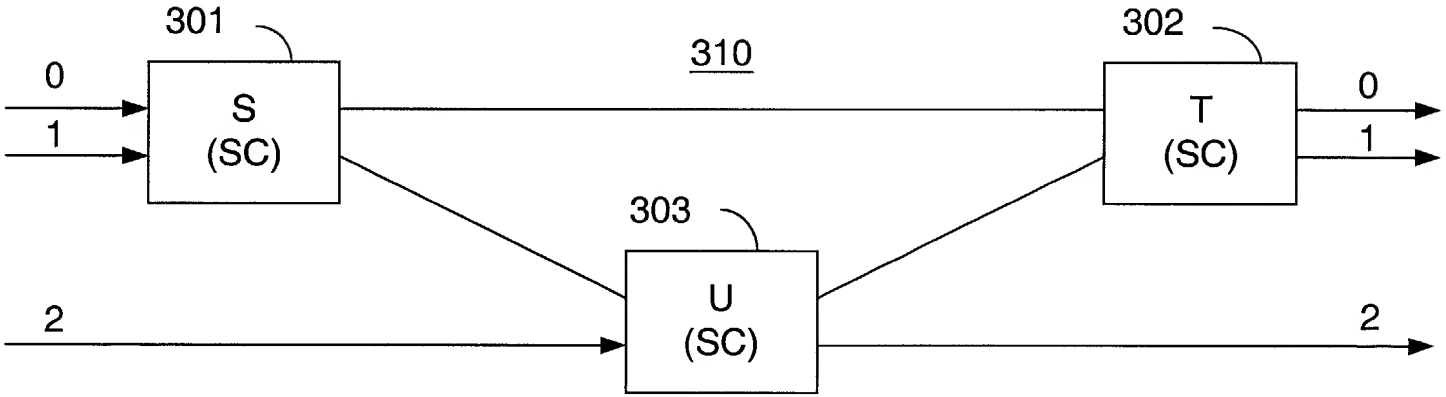



FIG. 3B

Page 30 of 2678

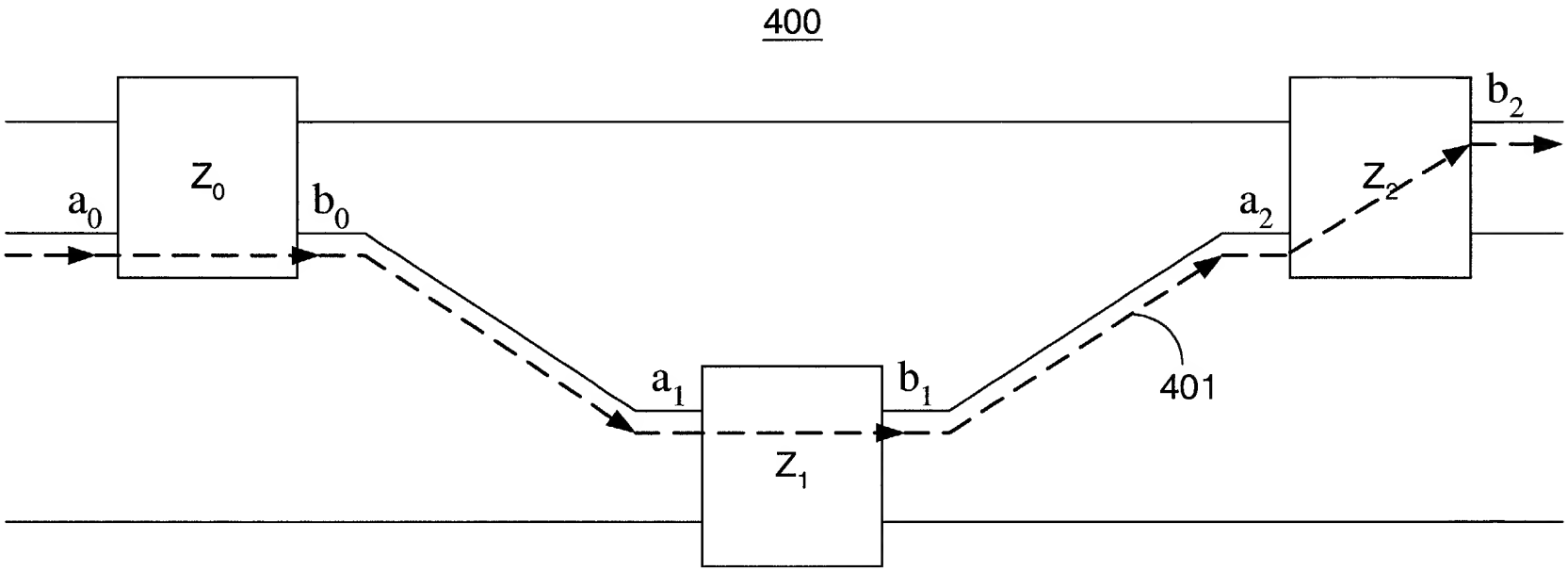



FIG. 4

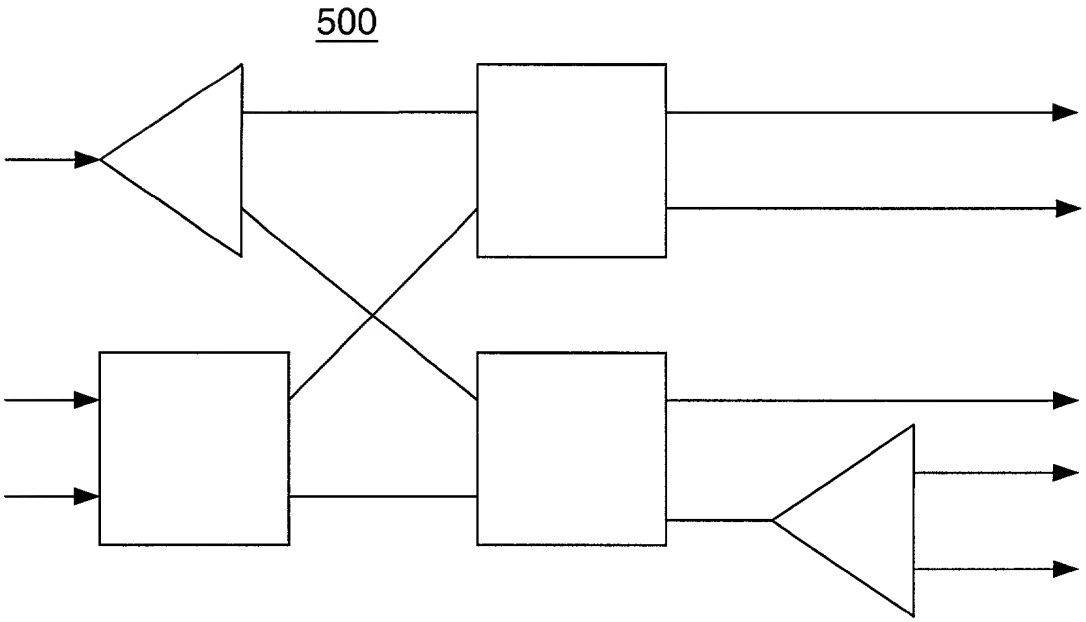



FIG. 5A

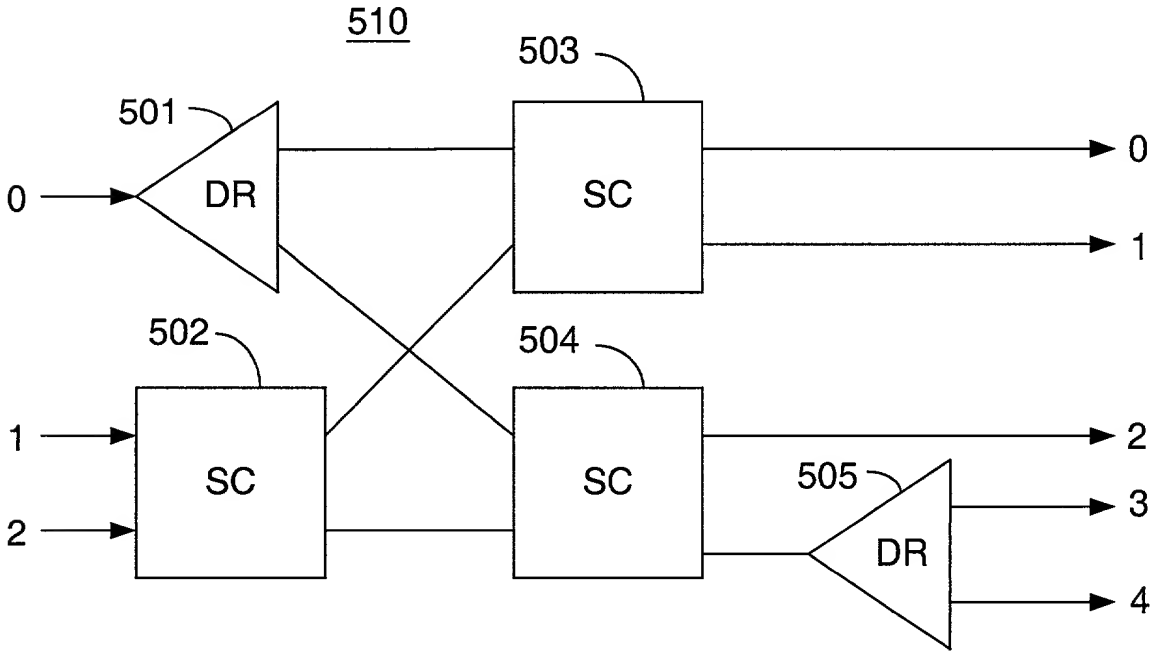



FIG. 5B

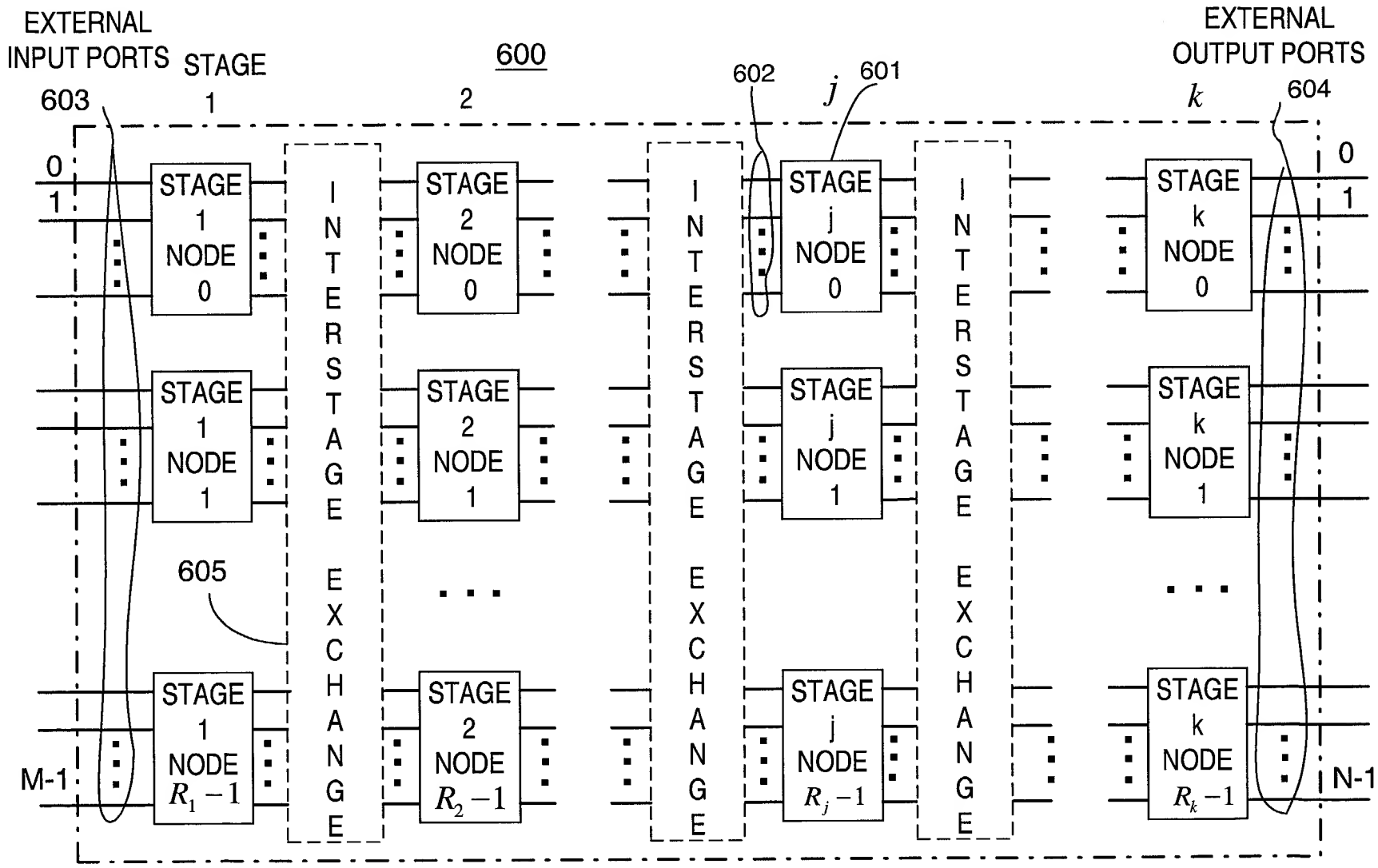

EXTERNAL
INPUT PORTS
STAGE
1
2
600
602
j
601
k
604
EXTERNAL
OUTPUT PORTS
603
0
1
M-1
STAGE 1 NODE 0
STAGE 1 NODE 1
STAGE 1 NODE $R_1 - 1$
INTERSTAGE EXCHANGE
STAGE 2 NODE 0
STAGE 2 NODE 1
STAGE 2 NODE $R_2 - 1$
INTERSTAGE EXCHANGE
STAGE j NODE 0
STAGE j NODE 1
STAGE j NODE $R_j - 1$
INTERSTAGE EXCHANGE
STAGE k NODE 0
STAGE k NODE 1
STAGE k NODE $R_k - 1$
0
1
N-1
605

FIG. 6A

Test Station

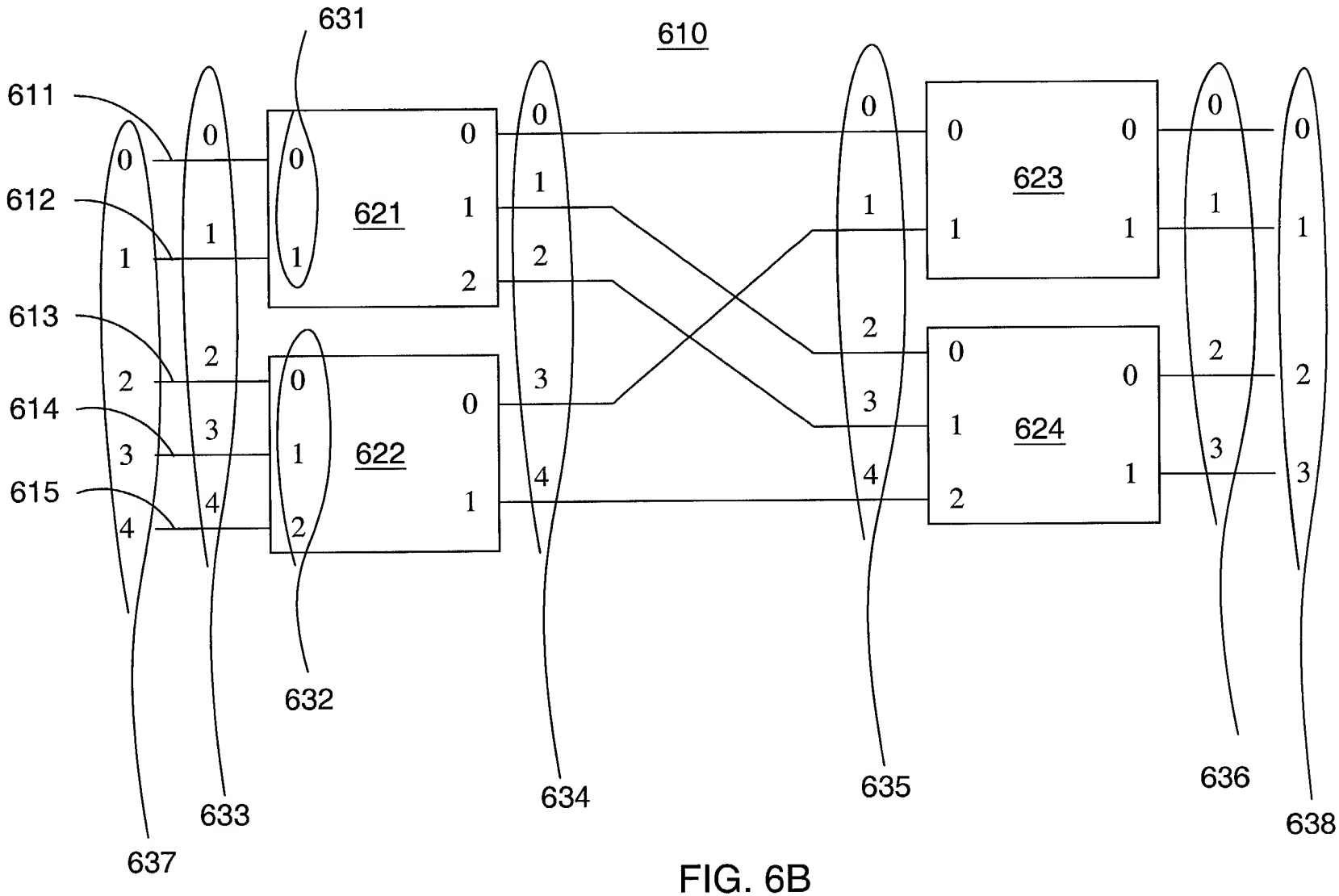



FIG. 6B

Tastor Zabtaid

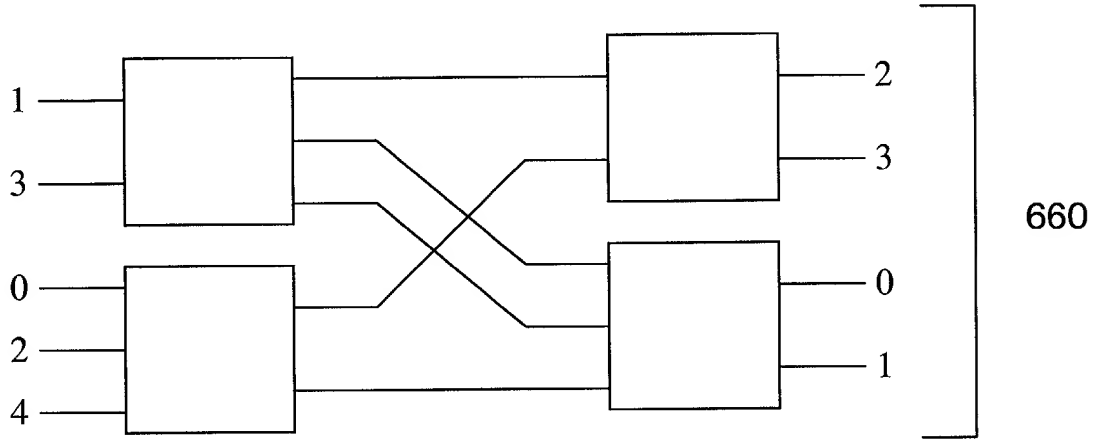



FIG. 6C

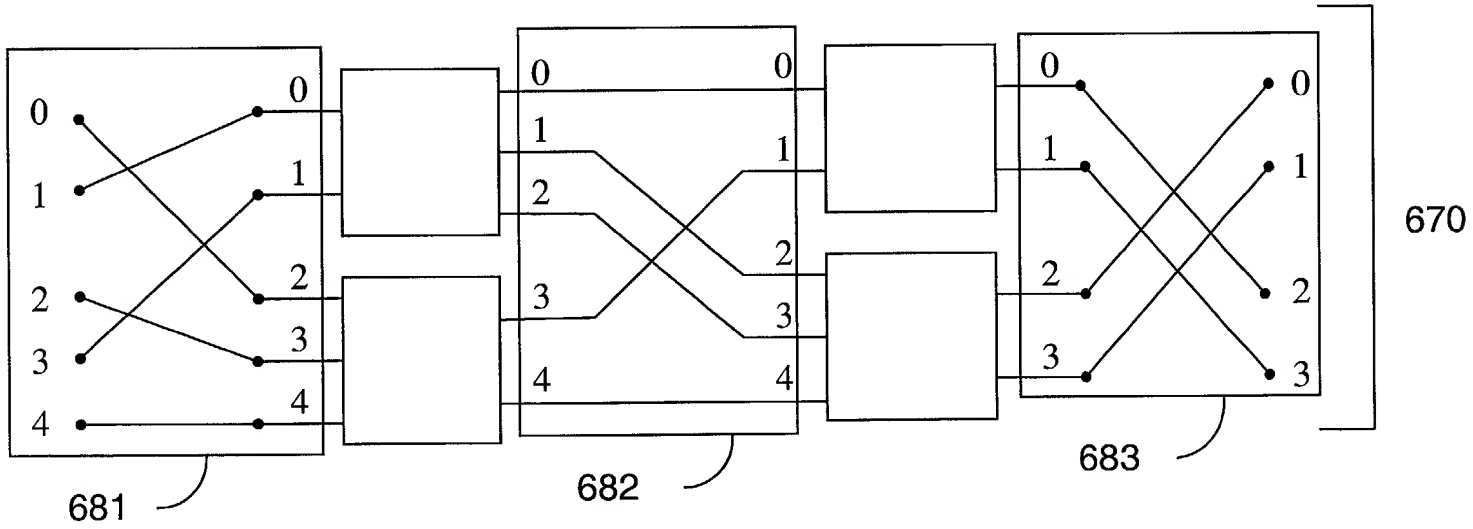



FIG. 6D

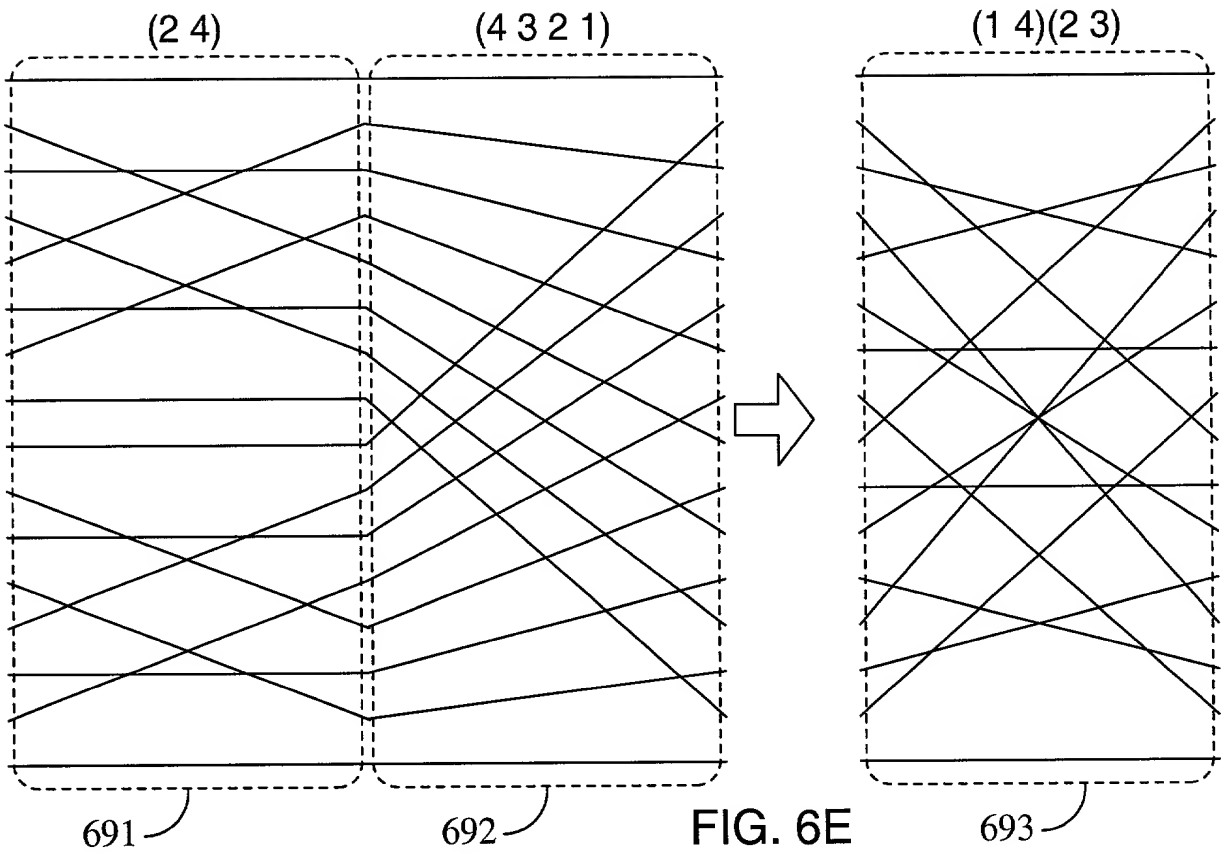



FIG. 6E

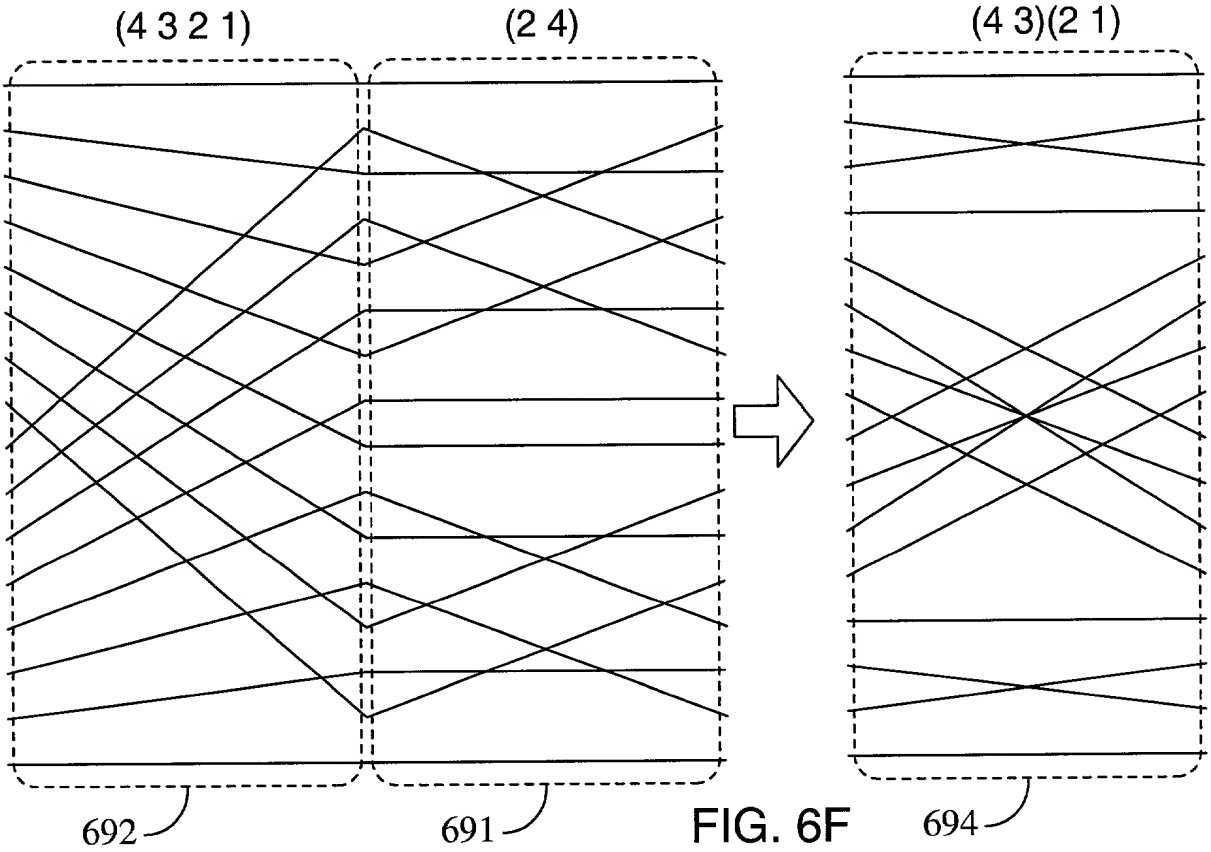



FIG. 6F

Patent Application Publication

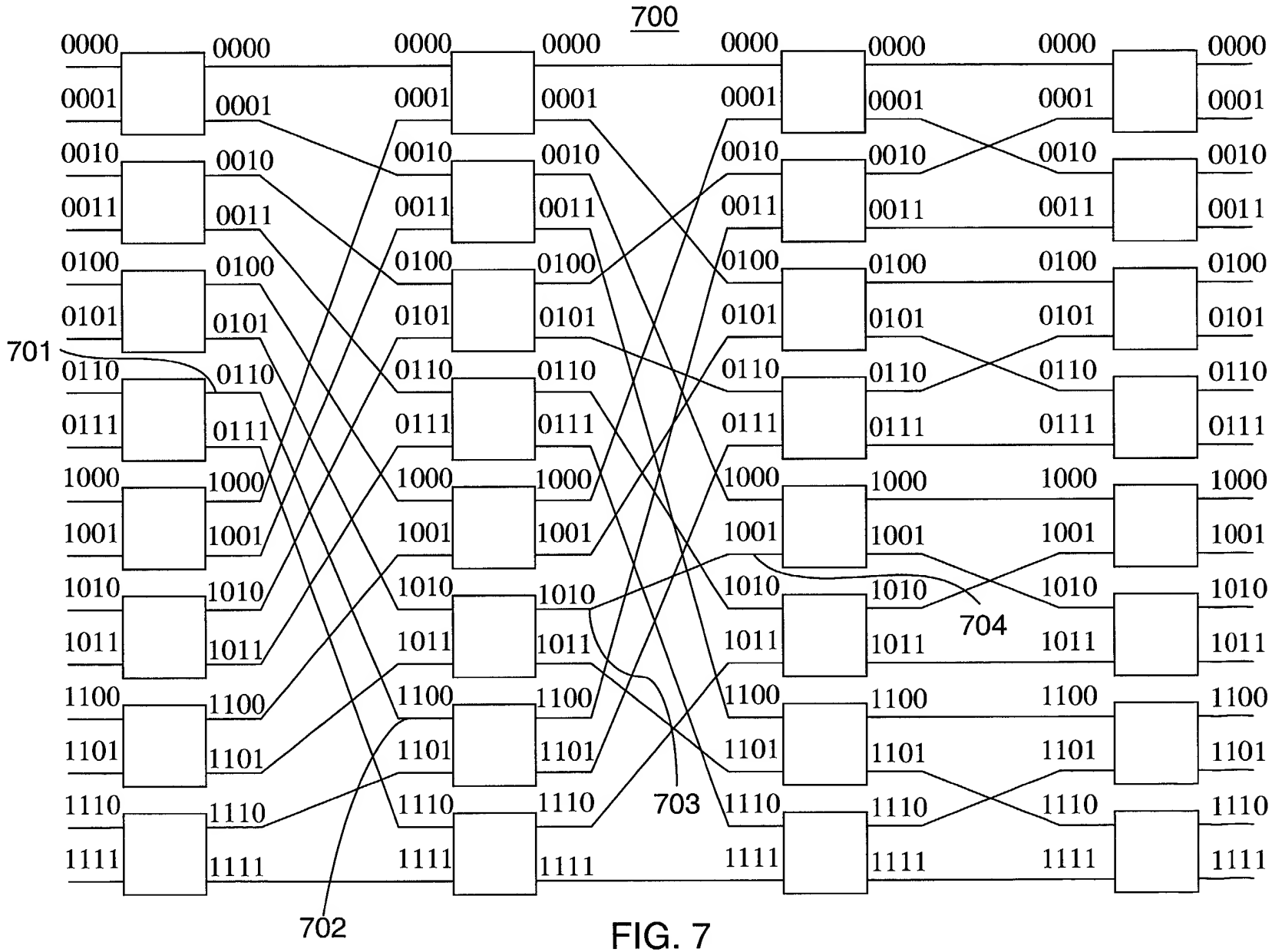



FIG. 7

800

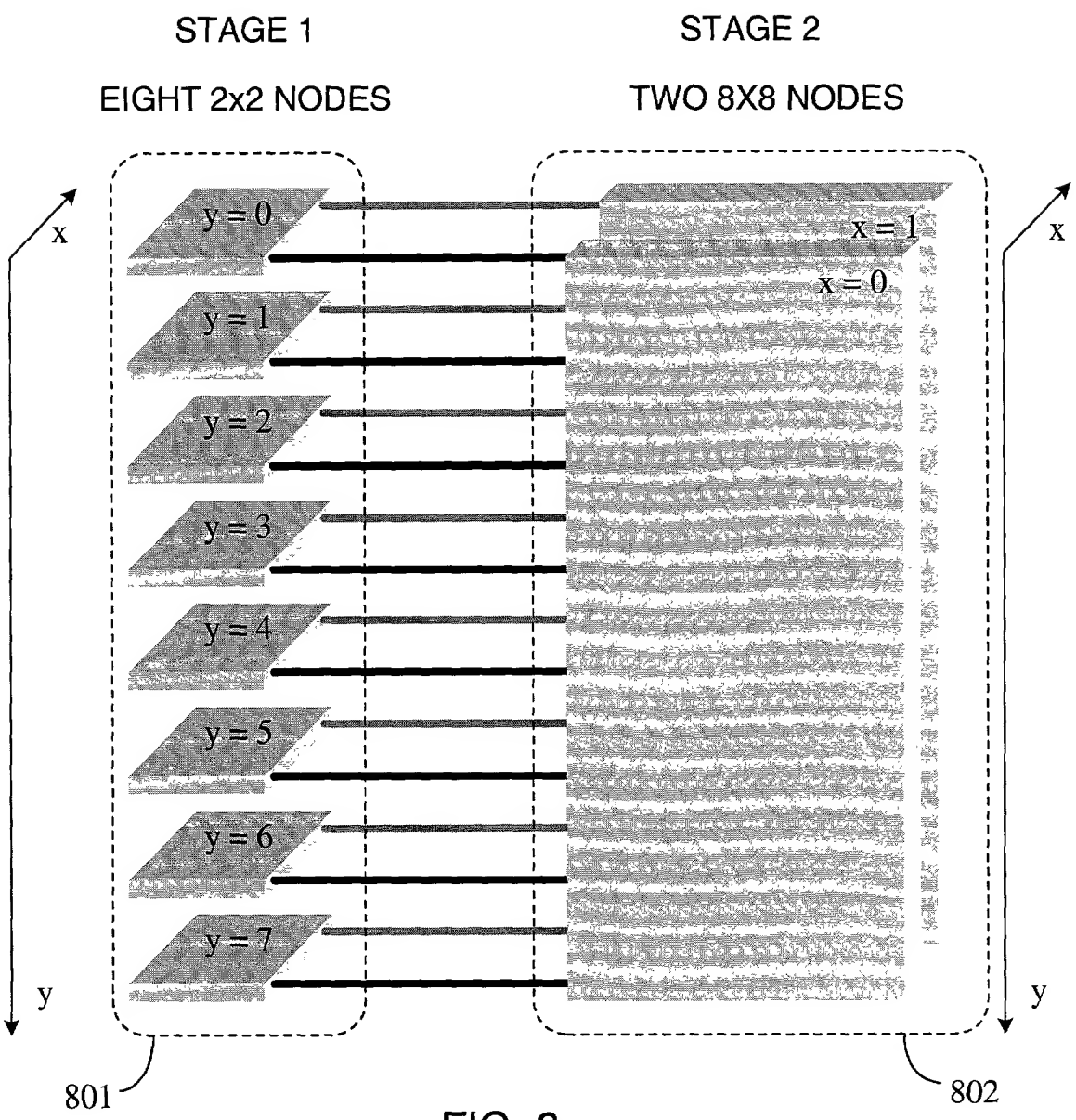

STAGE 1
EIGHT 2x2 NODES
STAGE 2
TWO 8X8 NODES
x
y
y = 0
y = 1
y = 2
y = 3
y = 4
y = 5
y = 6
y = 7
x = 1
x = 0
x
y
801
802

FIG. 8

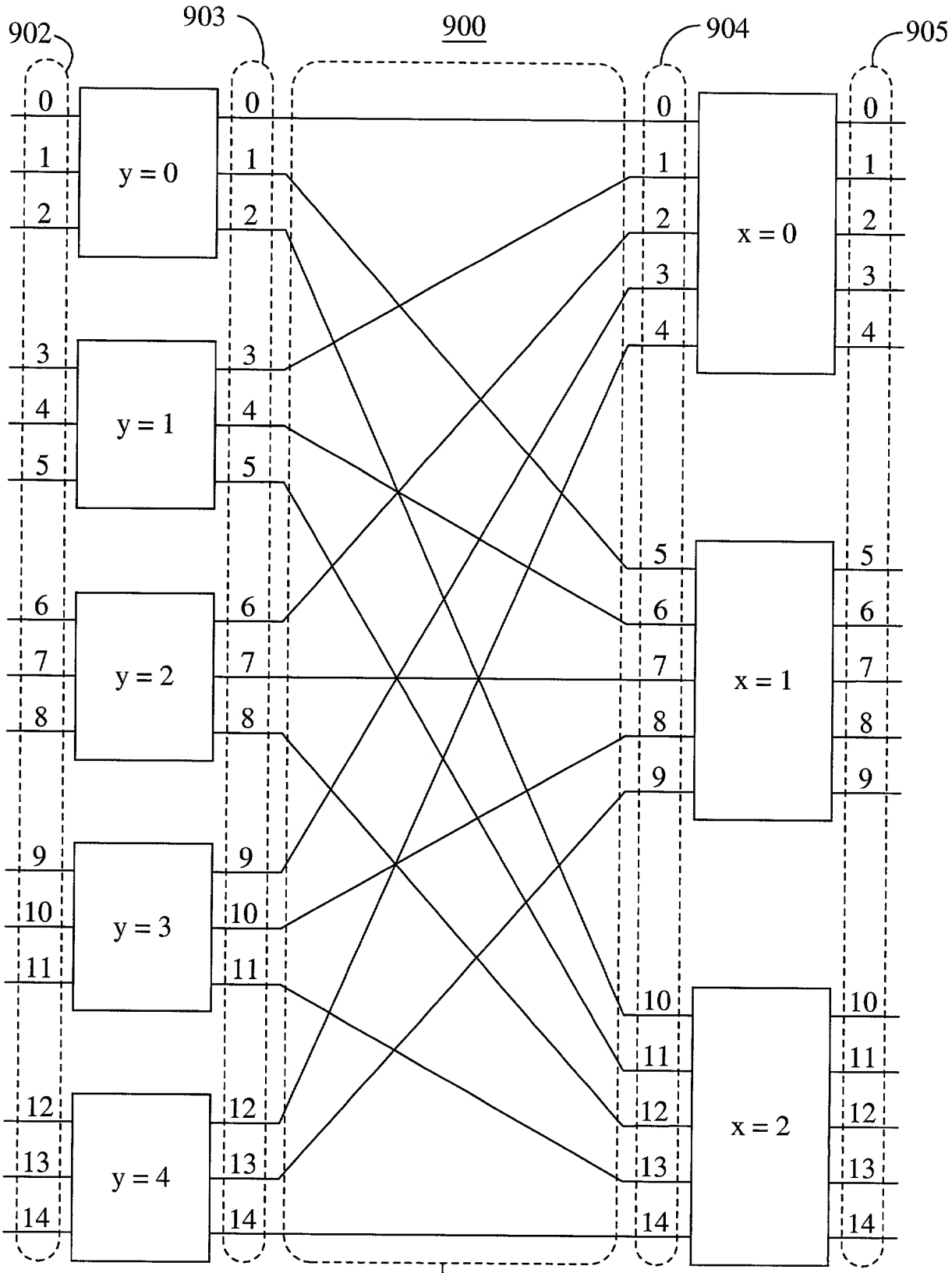

902
903
900
904
905
y = 0
y = 1
y = 2
y = 3
y = 4
x = 0
x = 1
x = 2
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
901

FIG. 9

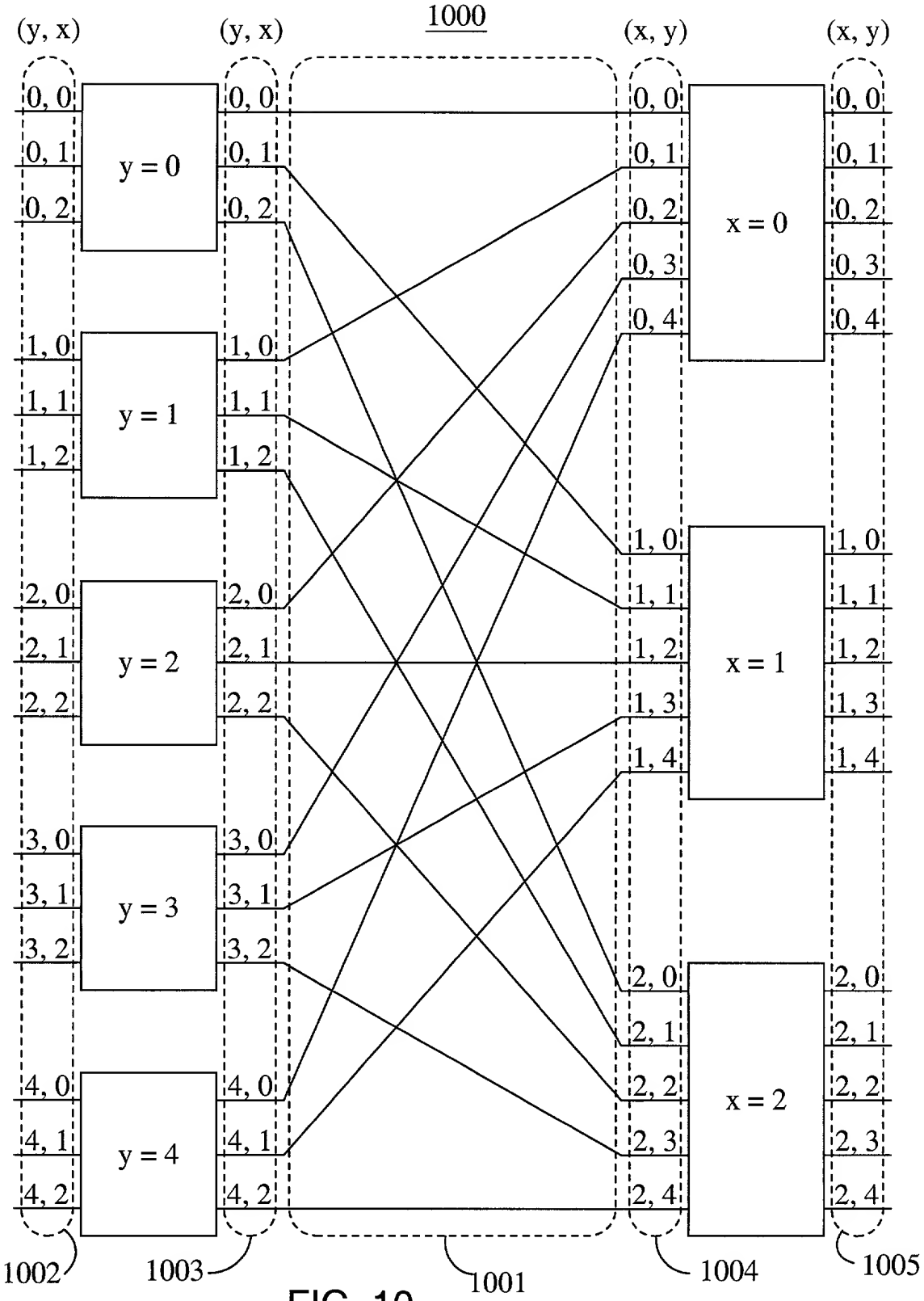

1000
(y, x)
(y, x)
(x, y)
(x, y)
0, 0
0, 1
0, 2
y = 0
1, 0
1, 1
1, 2
y = 1
2, 0
2, 1
2, 2
y = 2
3, 0
3, 1
3, 2
y = 3
4, 0
4, 1
4, 2
y = 4
0, 3
0, 4
x = 0
1, 3
1, 4
x = 1
2, 3
2, 4
x = 2
1002
1003
1001
1004
1005

FIG. 10

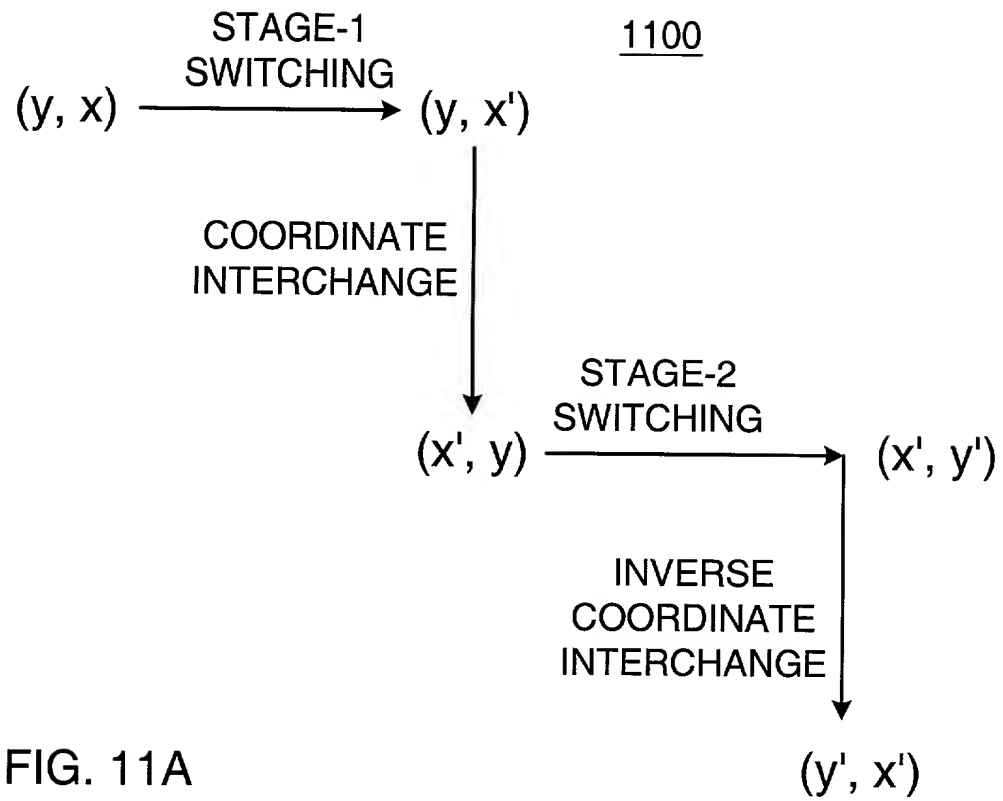



FIG. 11A

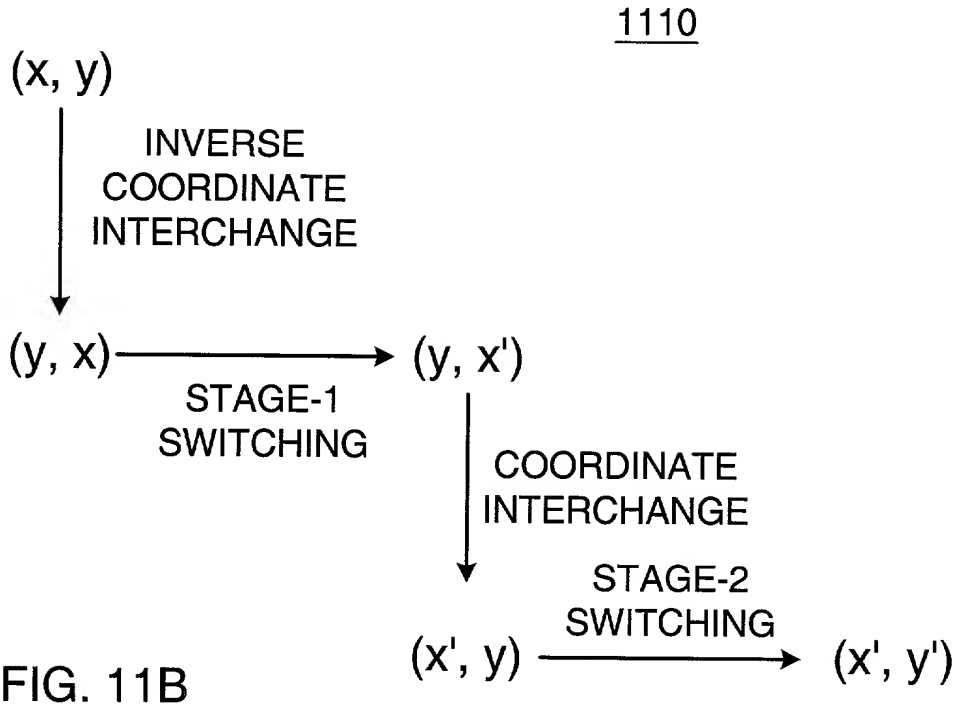



FIG. 11B

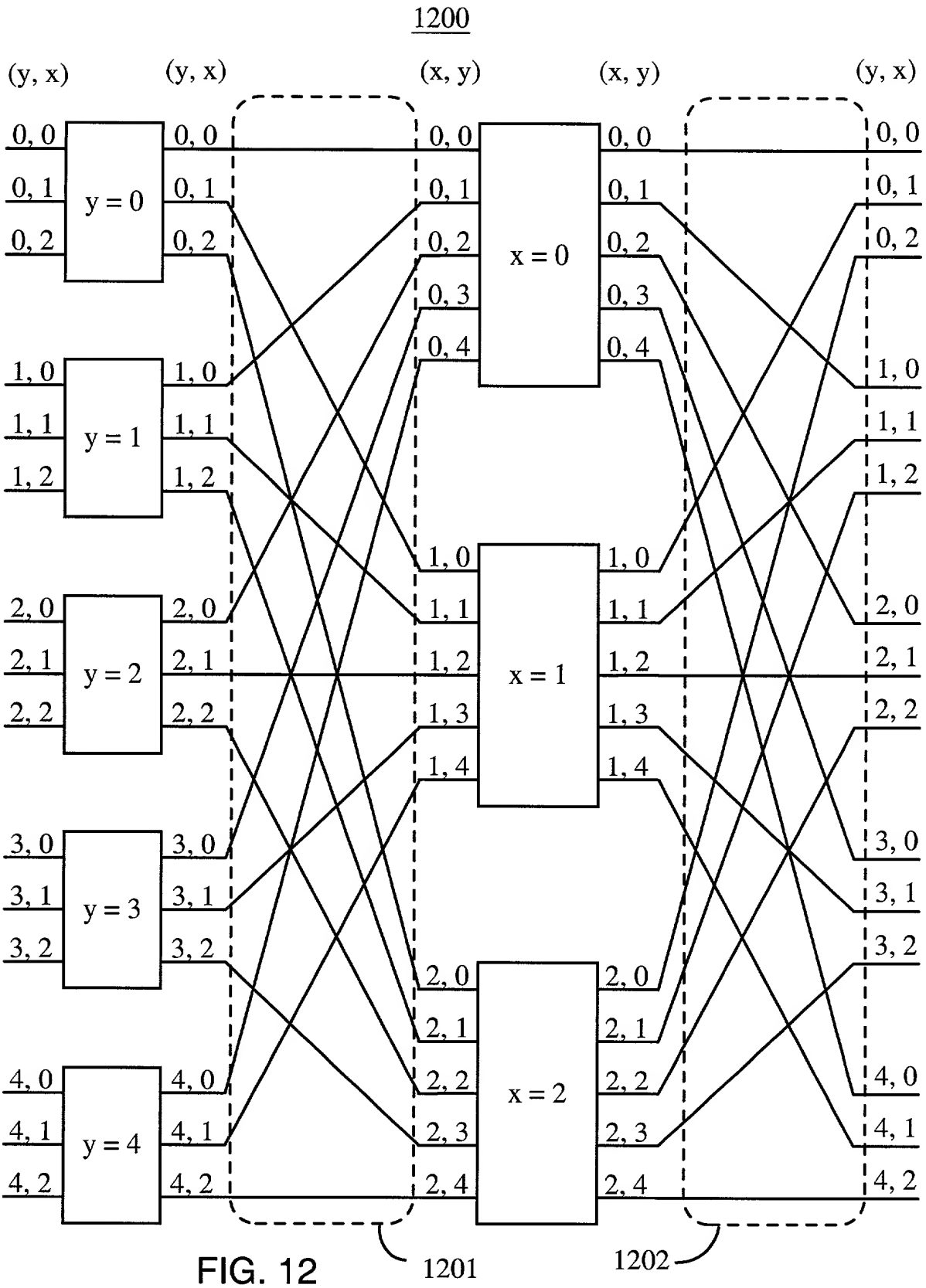

1200
(y, x)
(y, x)
(x, y)
(x, y)
(y, x)
0, 0
0, 1
0, 2
y = 0
1, 0
1, 1
1, 2
y = 1
2, 0
2, 1
2, 2
y = 2
3, 0
3, 1
3, 2
y = 3
4, 0
4, 1
4, 2
y = 4
x = 0
x = 1
x = 2
1201
1202

FIG. 12

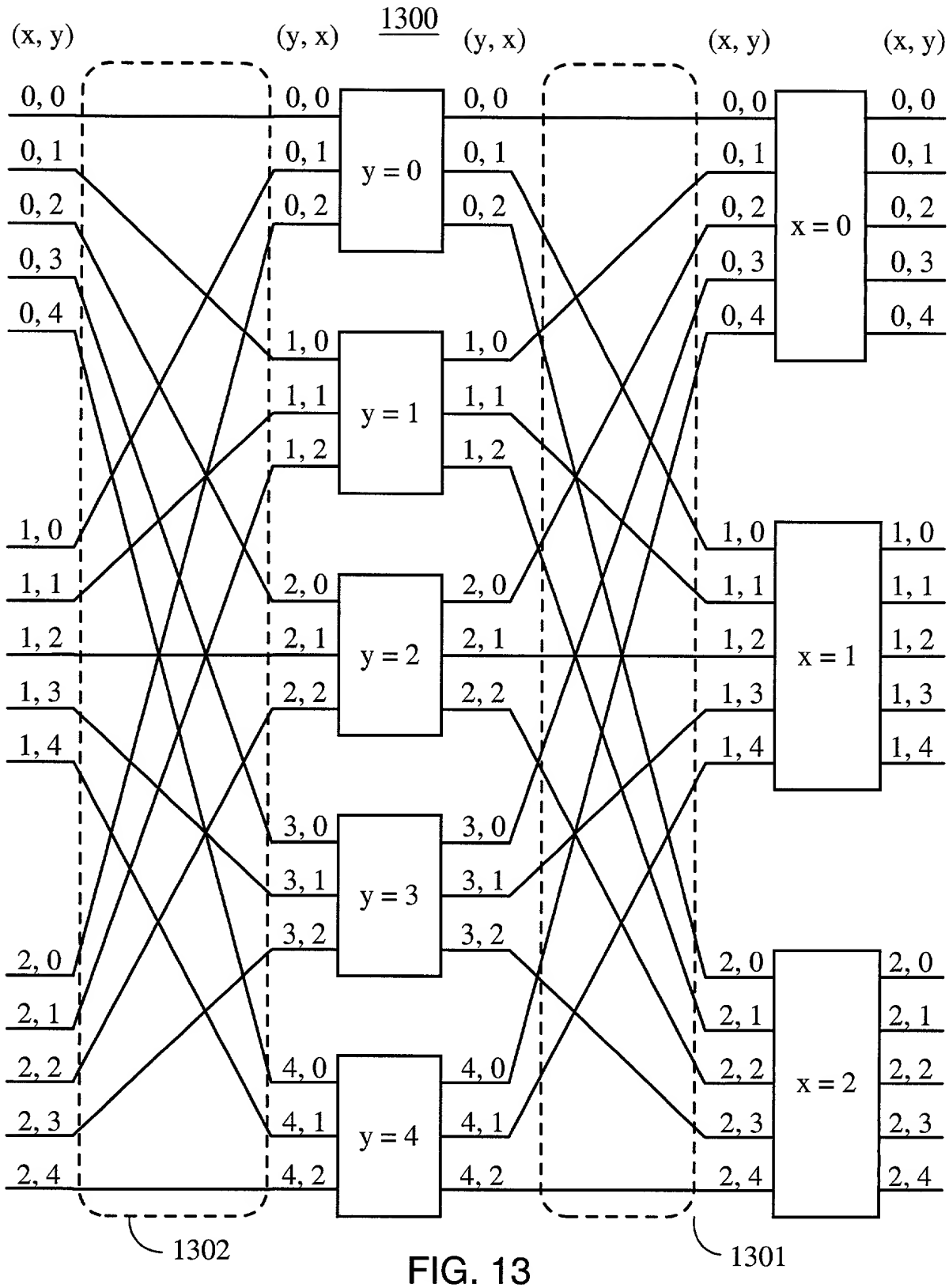
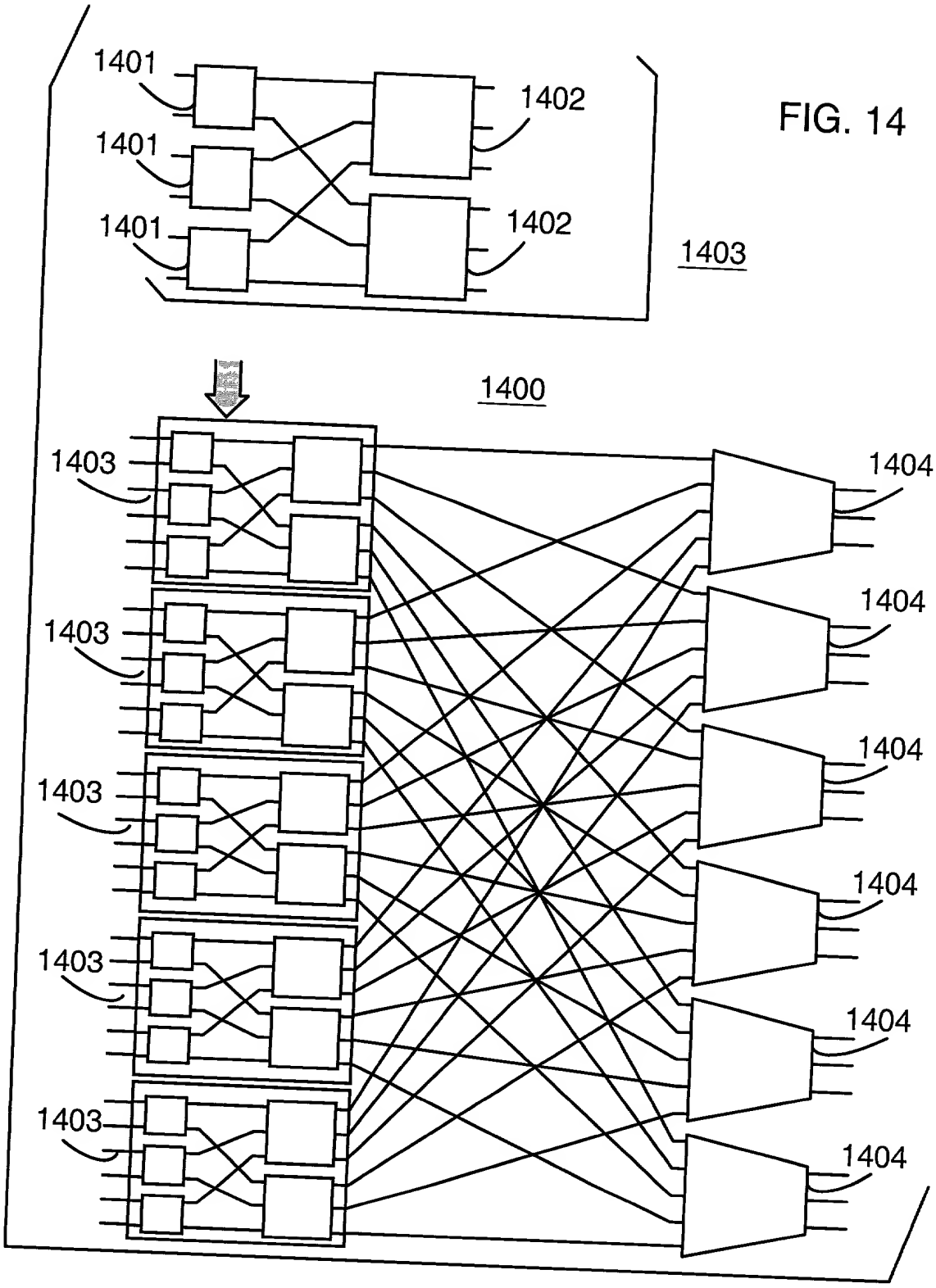

1300
(x, y)
(y, x)
(y, x)
(x, y)
(x, y)
0, 0
0, 1
0, 2
0, 3
0, 4
1, 0
1, 1
1, 2
1, 3
1, 4
2, 0
2, 1
2, 2
2, 3
2, 4
y = 0
y = 1
y = 2
y = 3
y = 4
x = 0
x = 1
x = 2
1302
1301

FIG. 13


1401
1401
1401
1402
1402
1403
1400
1403
1403
1403
1403
1403
1404
1404
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1404
1404
1404

FIG. 14

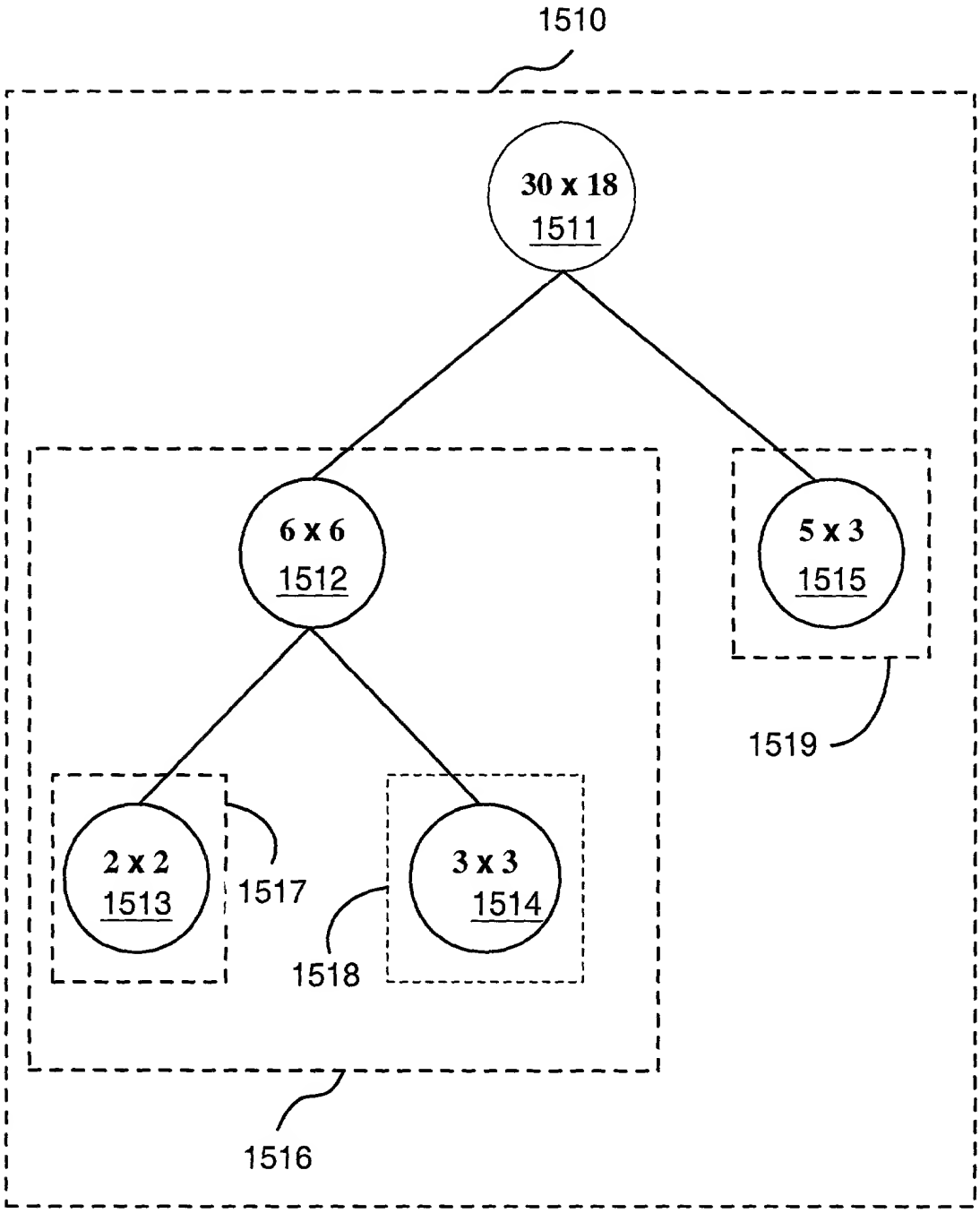

1510
30 x 18
1511
6 x 6
1512
5 x 3
1515
1519
2 x 2
1513
1517
3 x 3
1514
1518
1516

FIG. 15

TOSTSD-2S8T8S4S

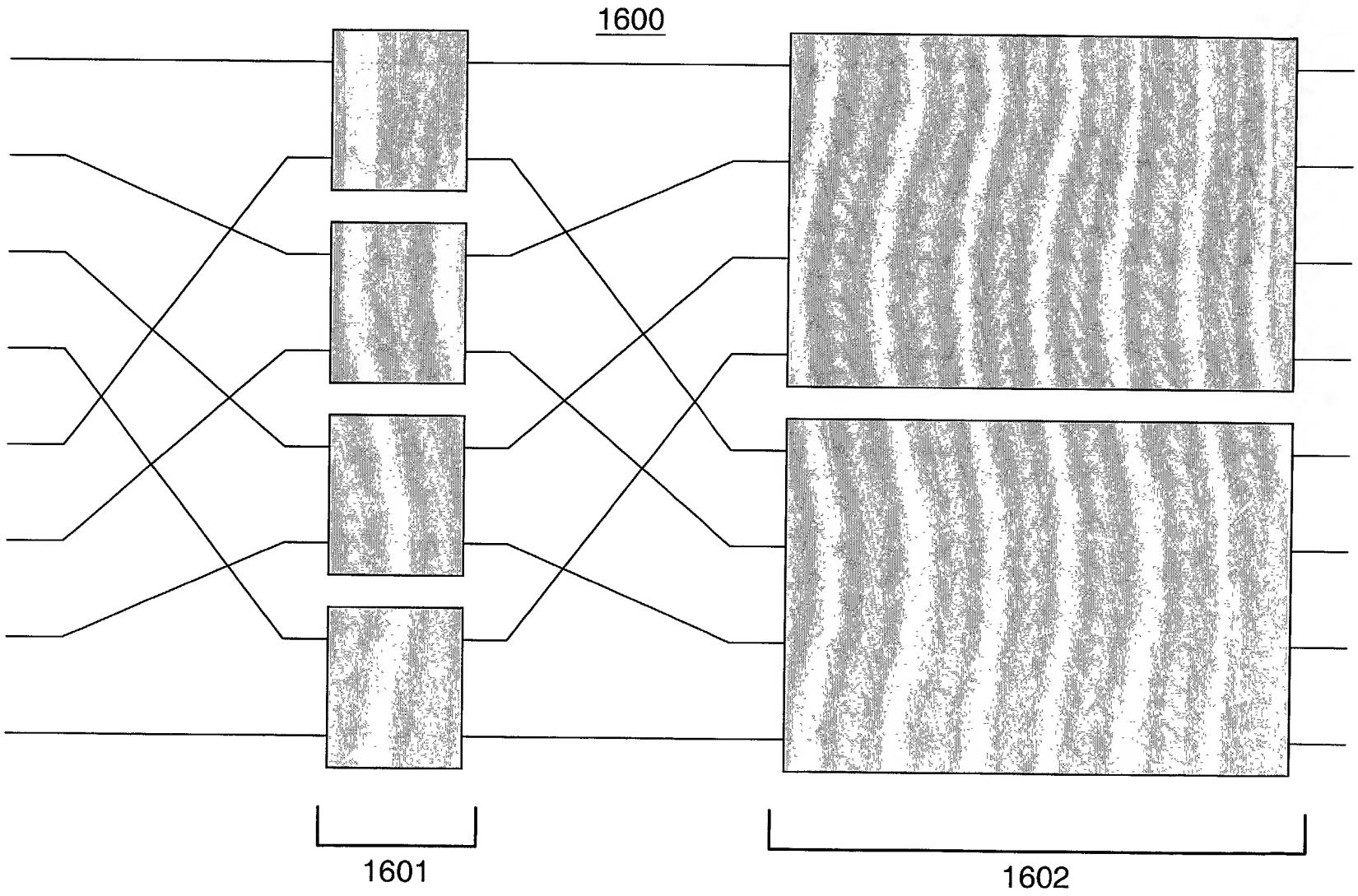



FIG. 16

PCT/US2004/000000

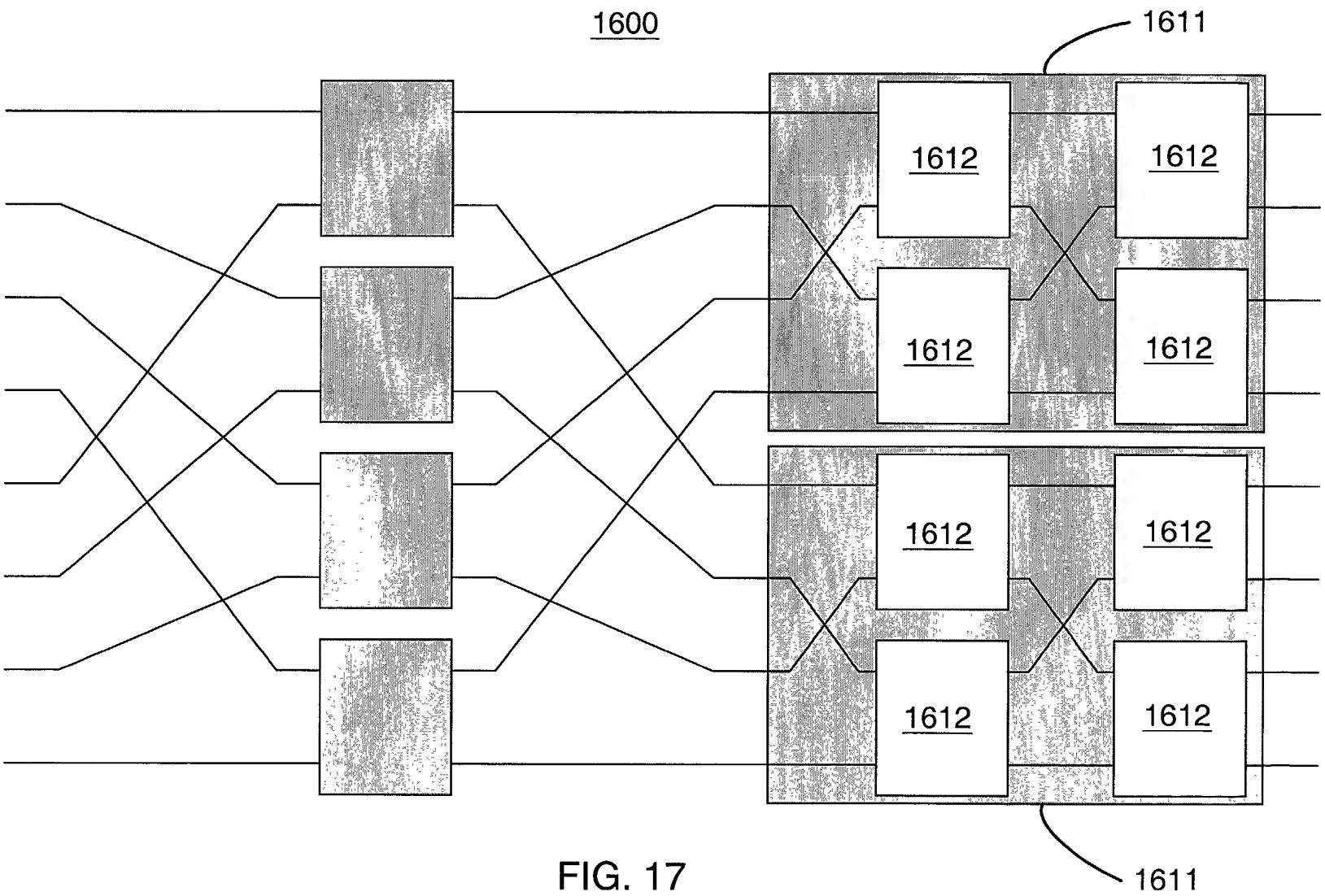



FIG. 17

PCT/SG2004/000340

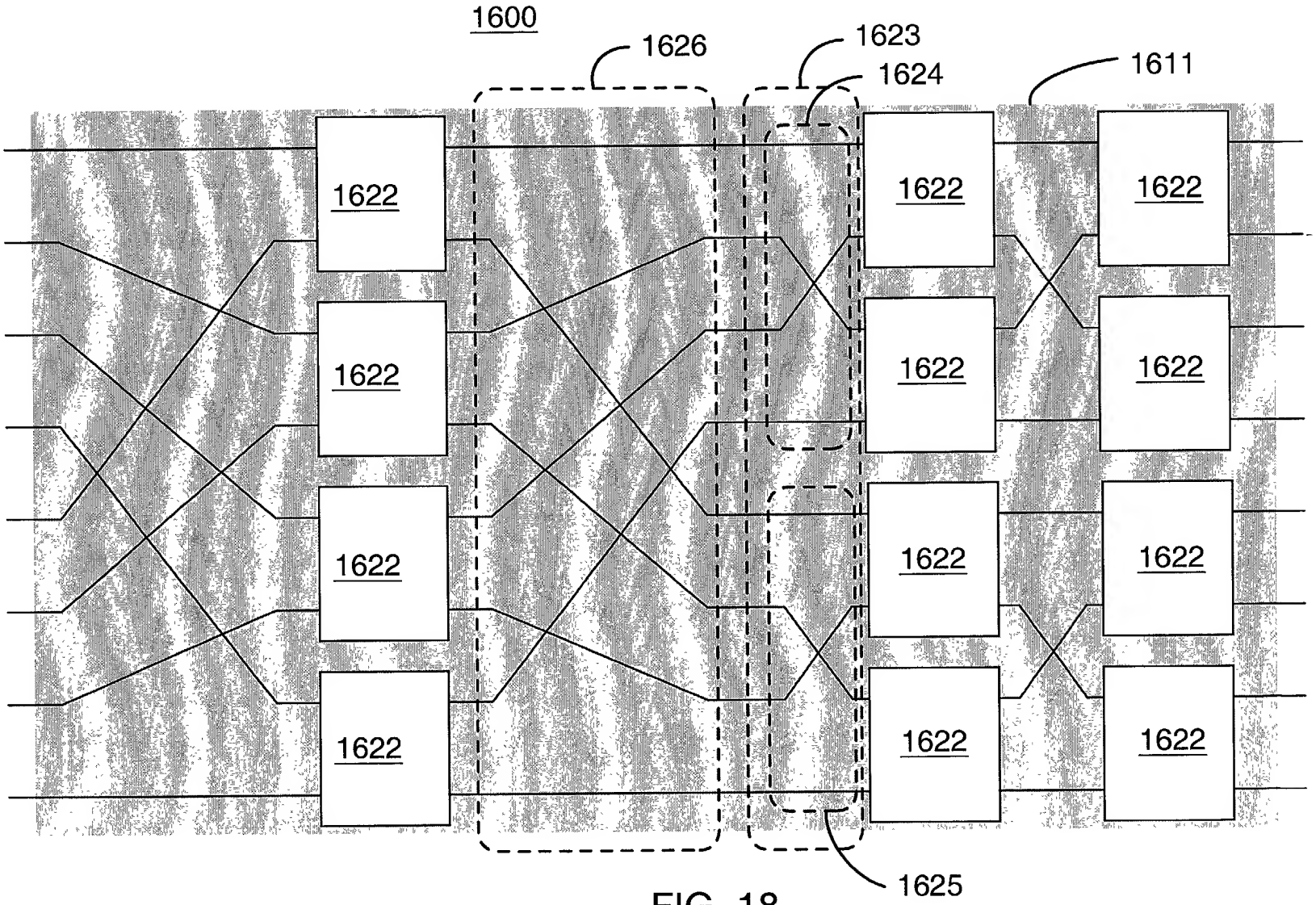



FIG. 18

PUBLISHED

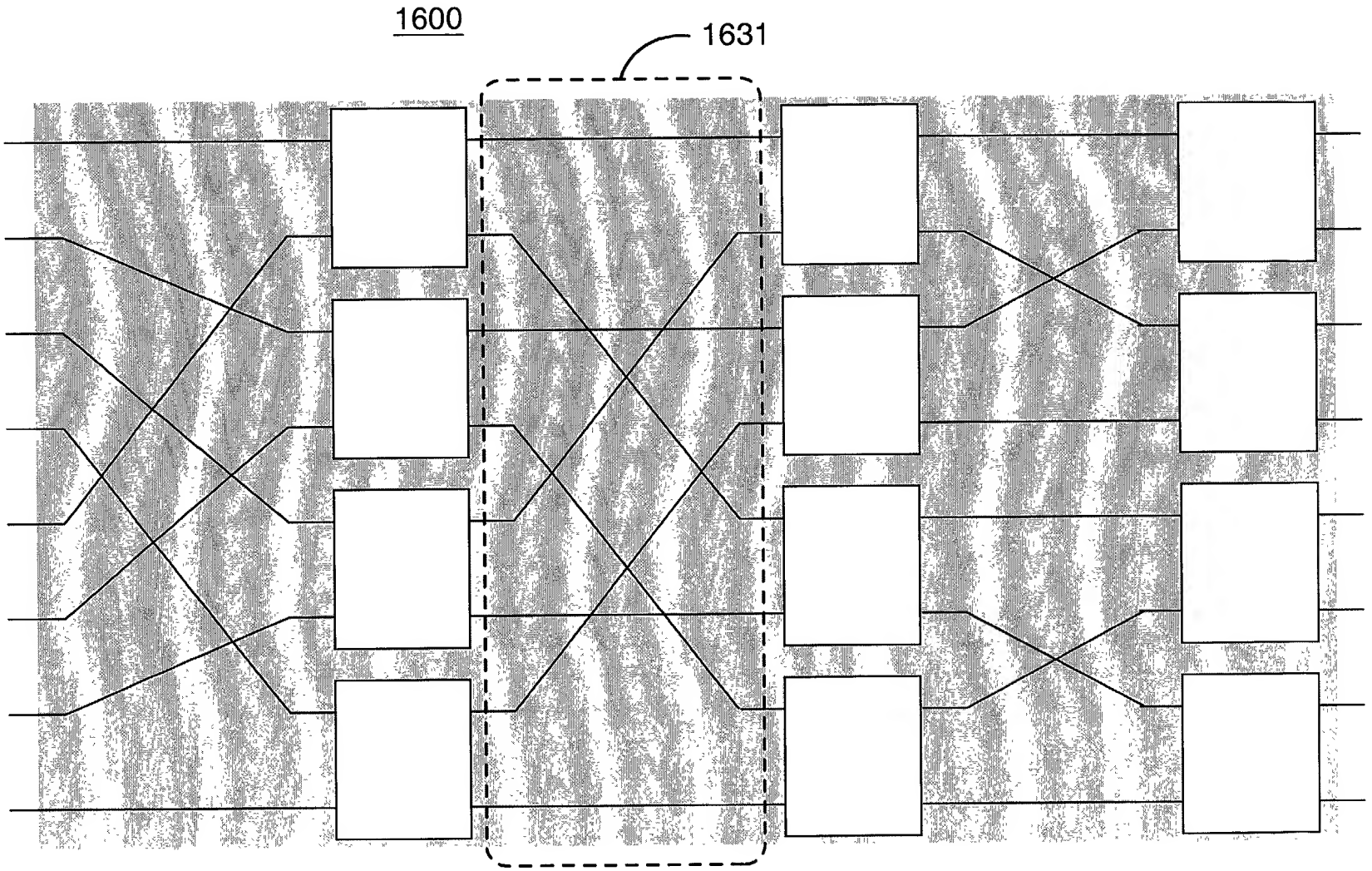



FIG. 19

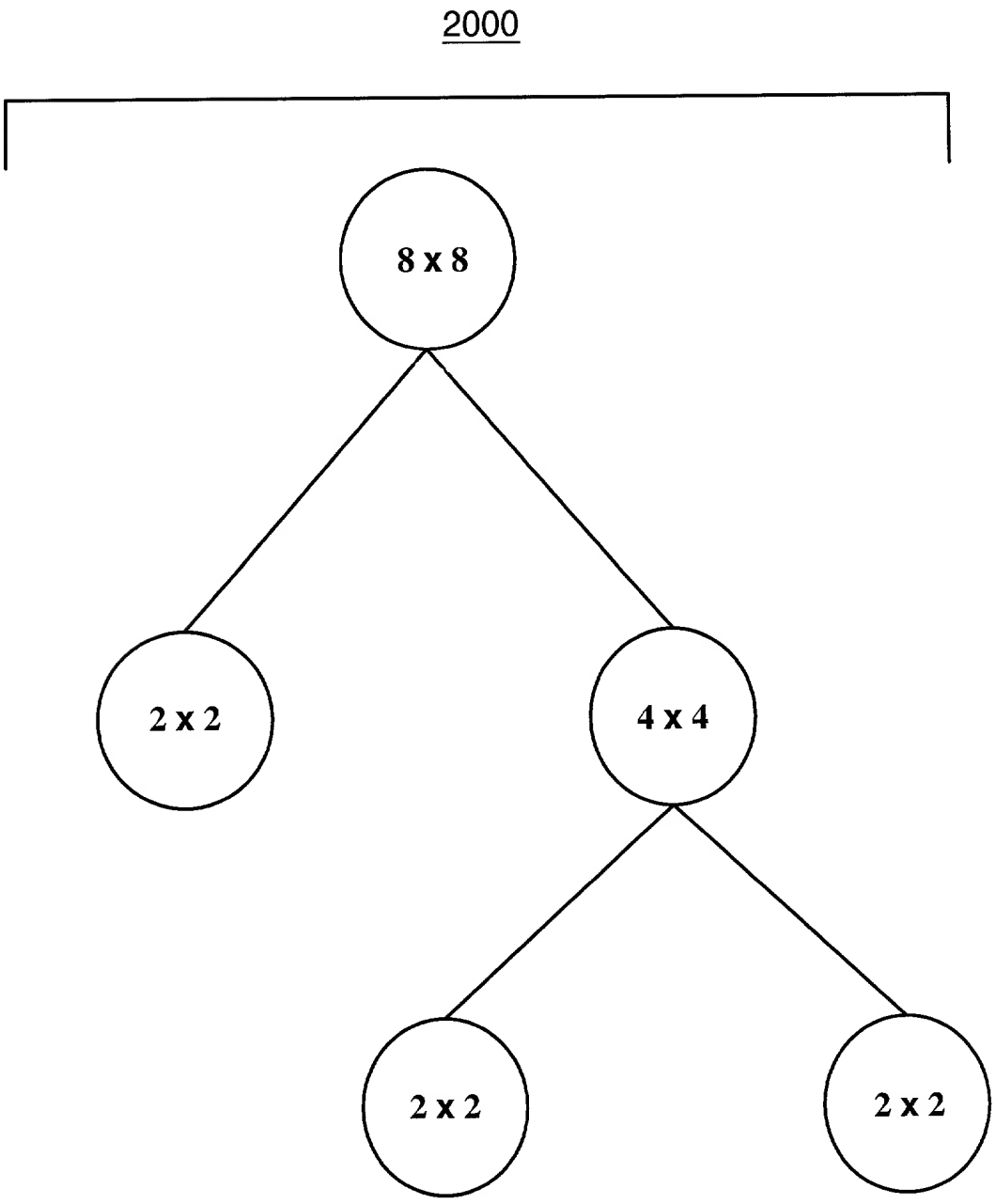



FIG. 20

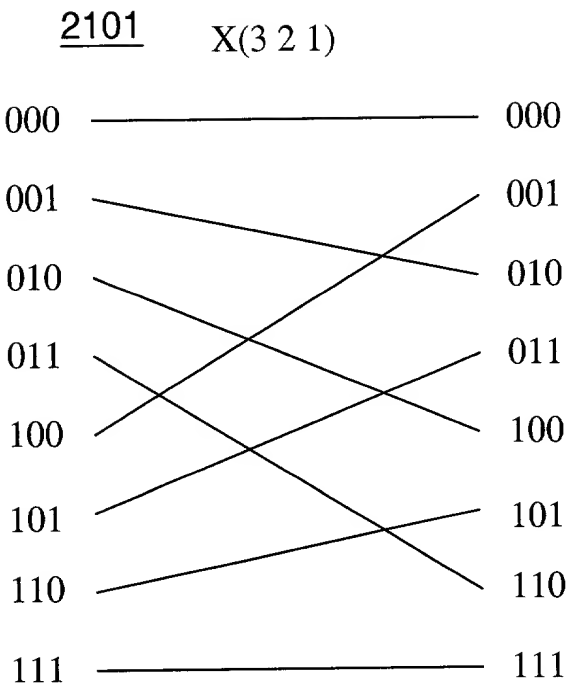



FIG. 21A

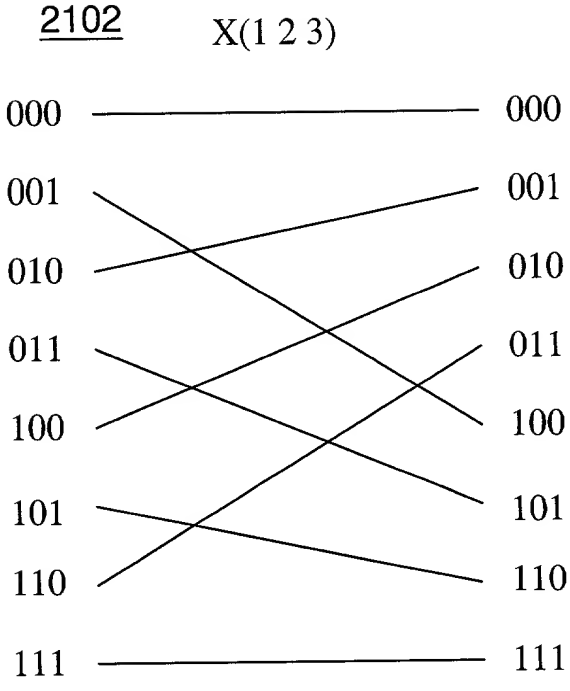



FIG. 21B

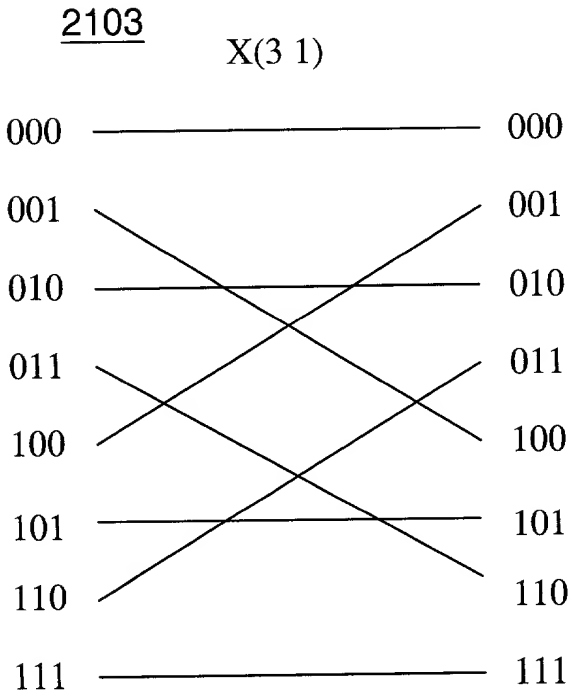



FIG. 21C

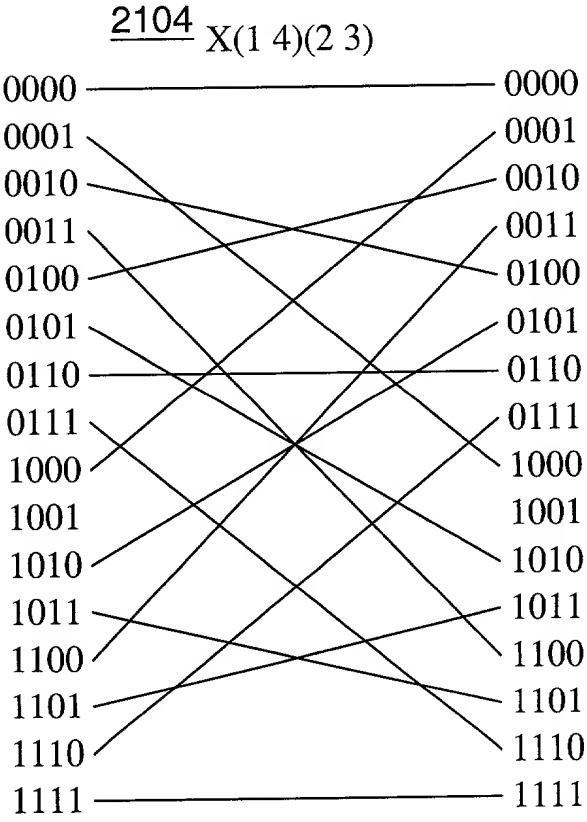
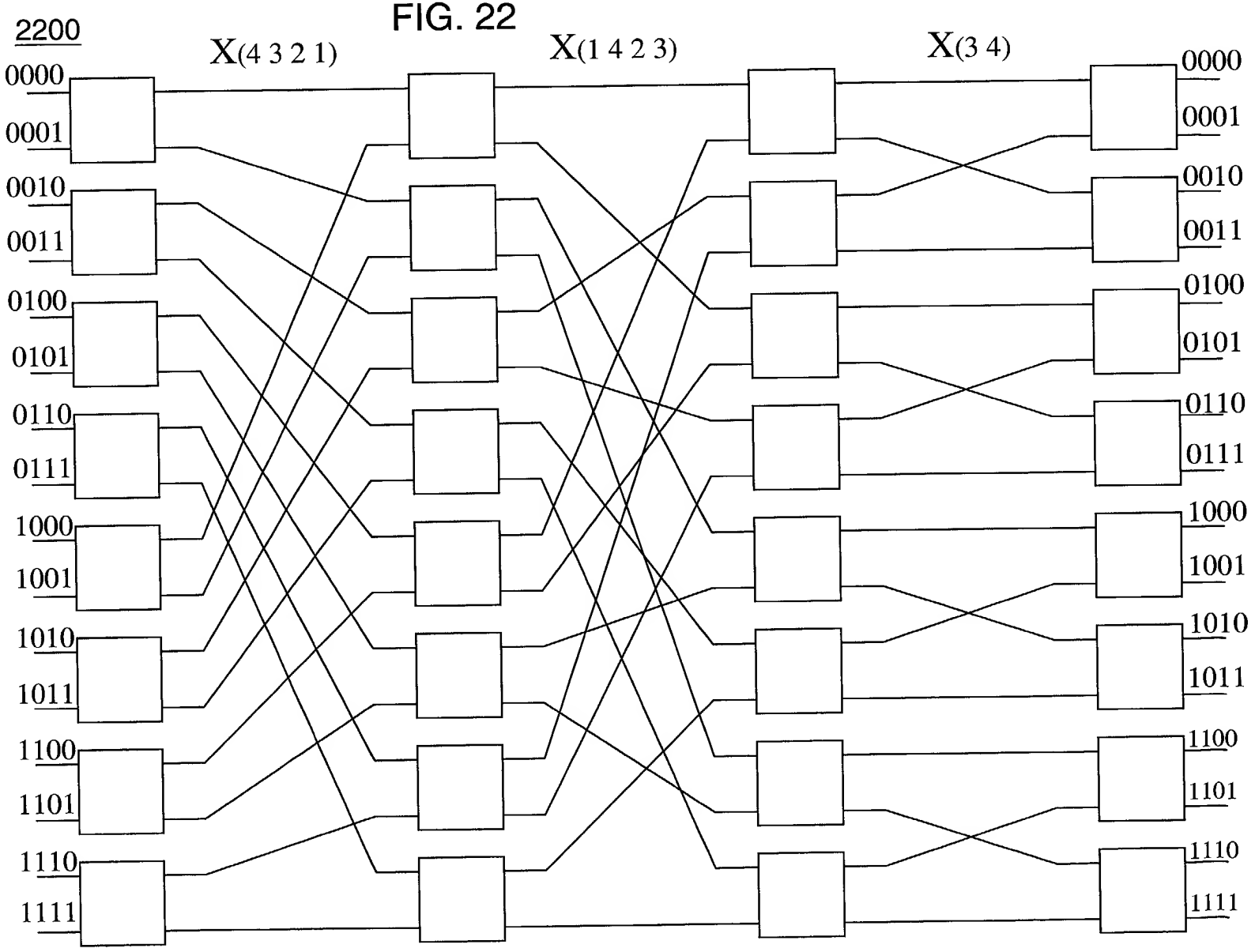



FIG. 21D

FIG. 22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X(1 4 2 3)
X(3 4)
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
0000
0001
0010
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0100
0101
0110
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1010
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1100
1101
1110
1111

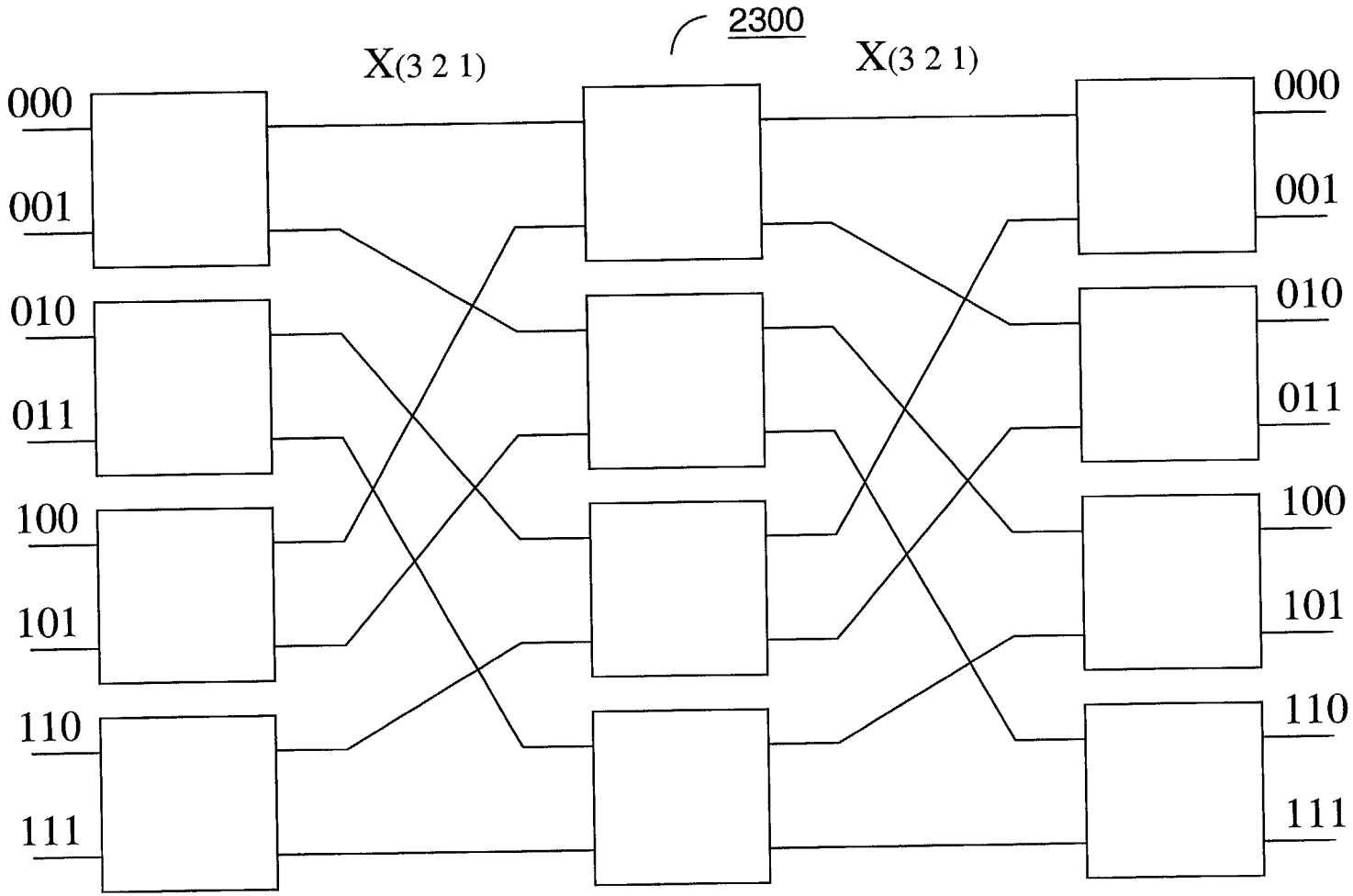

2300
X(3 2 1)
X(3 2 1)
000
001
010
011
100
101
110
111
000
001
010
011
100
101
110
111

FIG. 23

2400

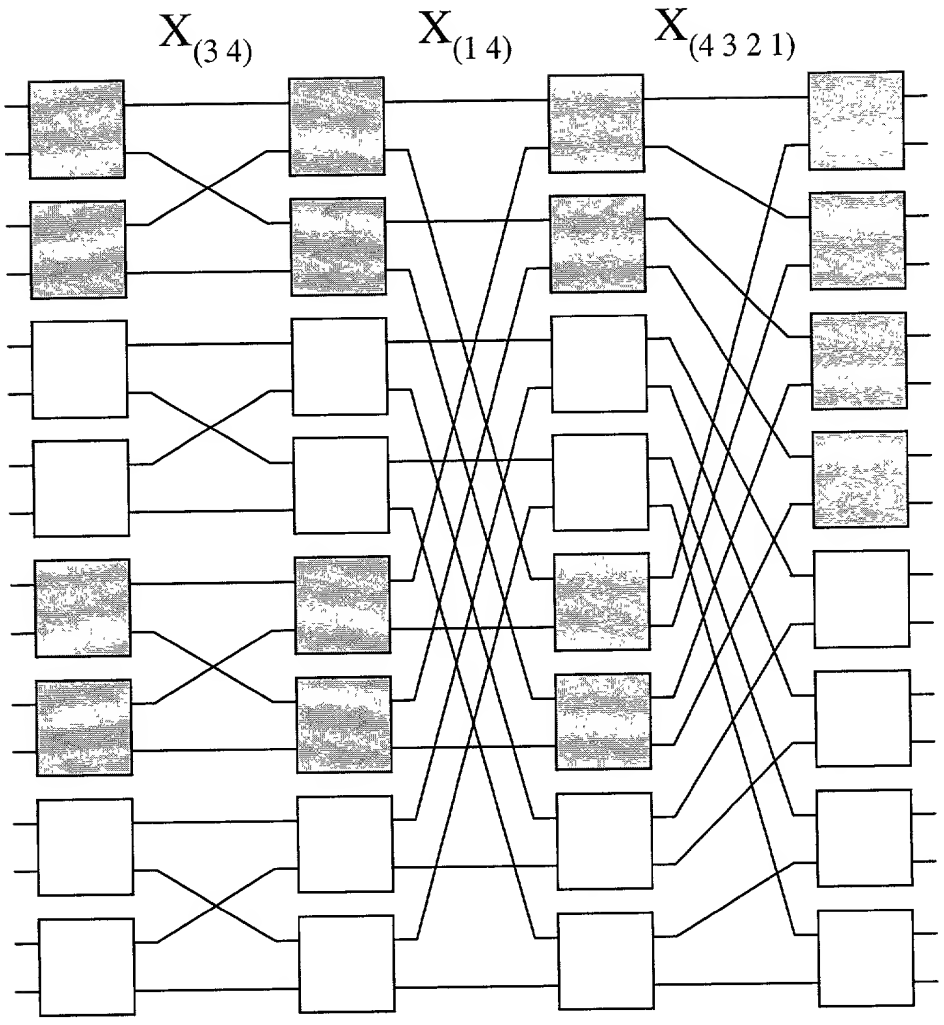



FIG. 24

FIG. 25

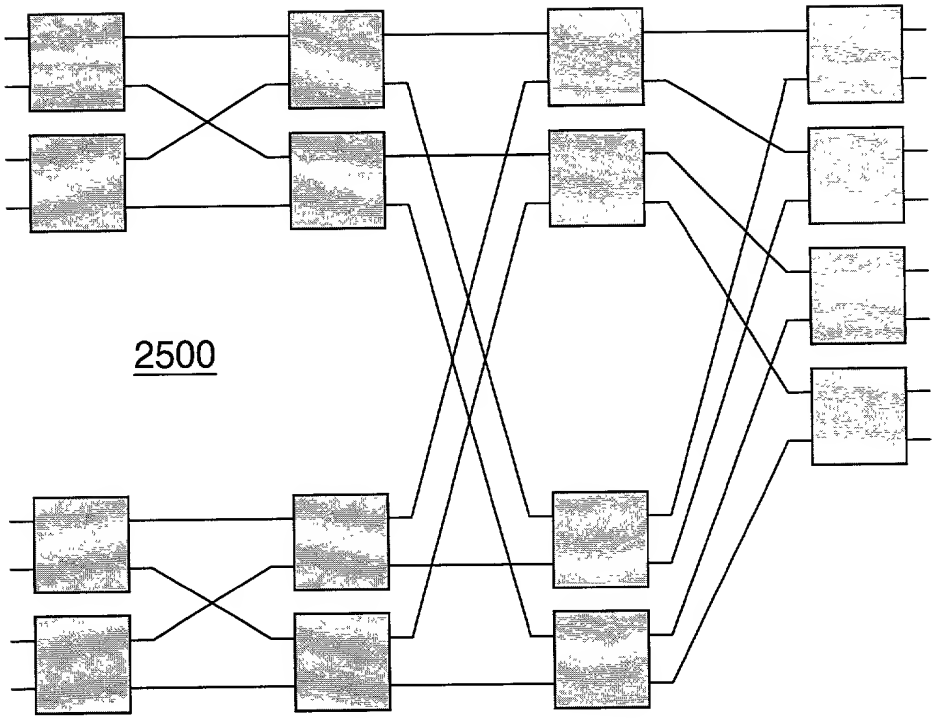
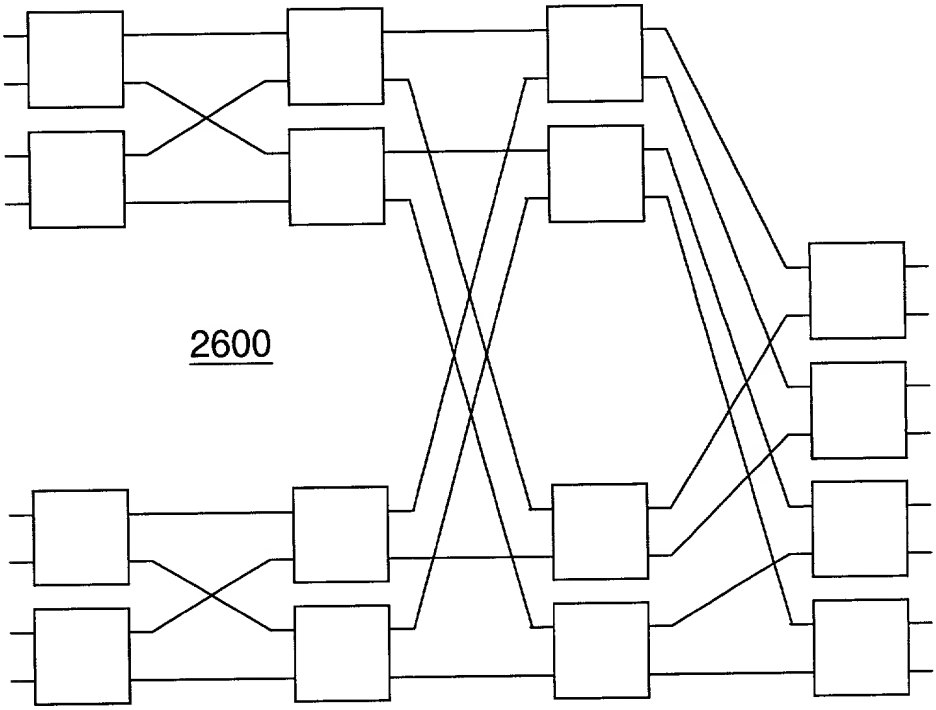



FIG. 26



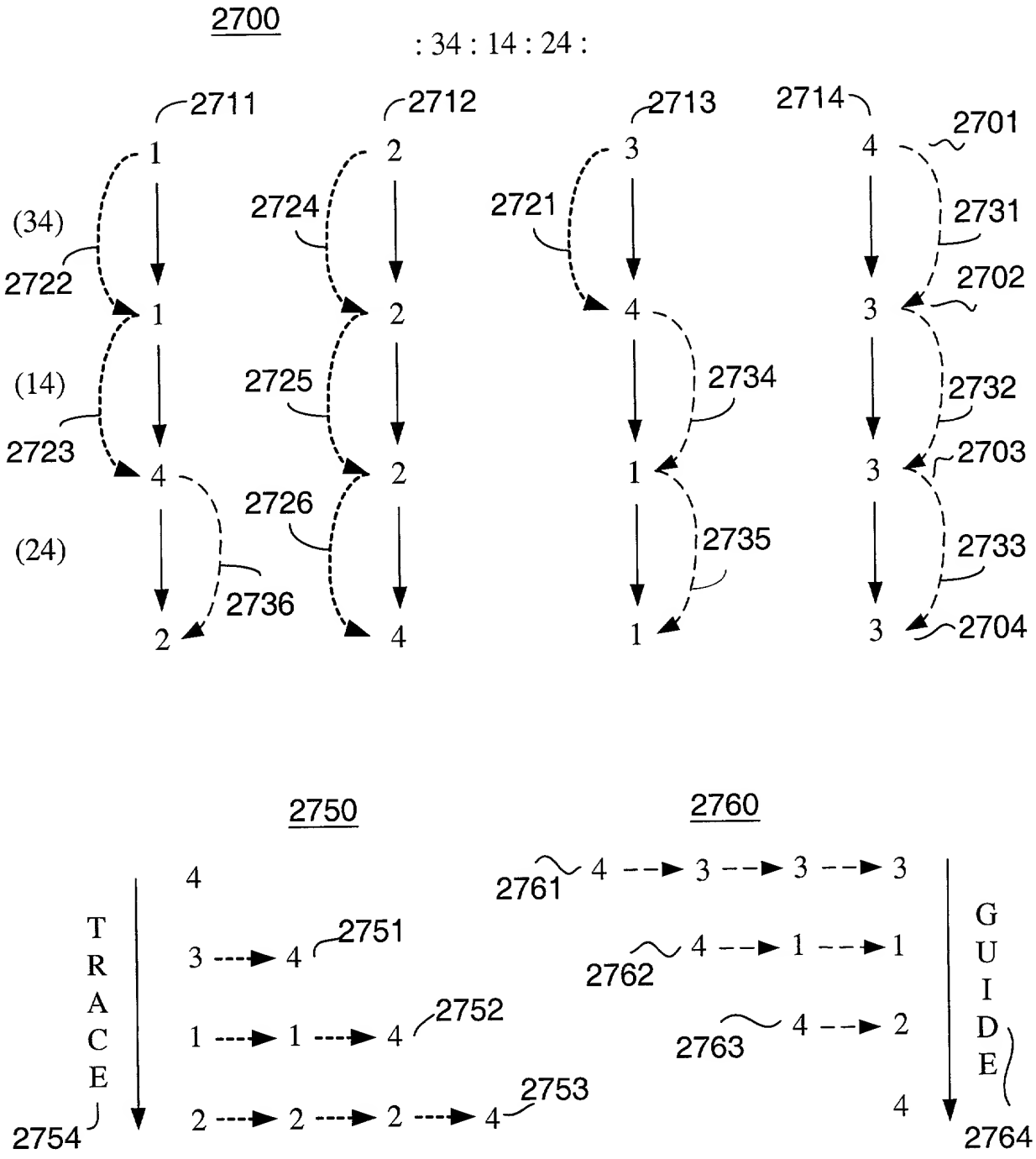

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FIG. 27

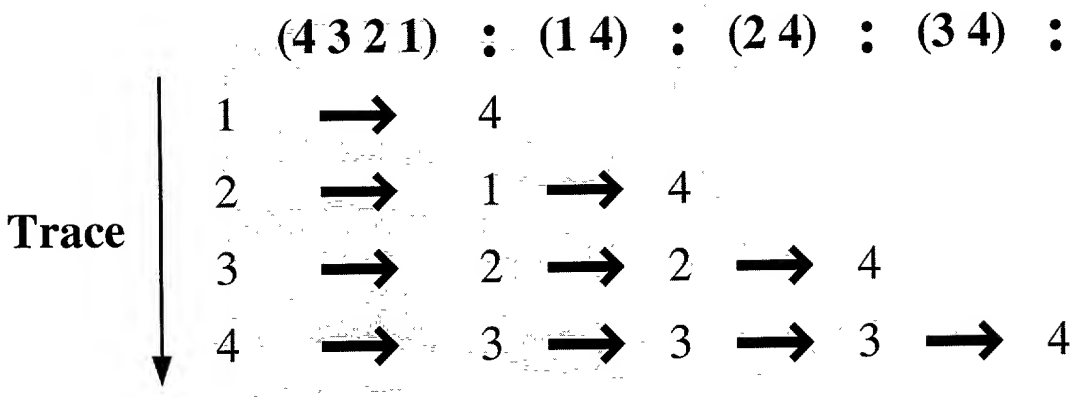



FIG. 28A

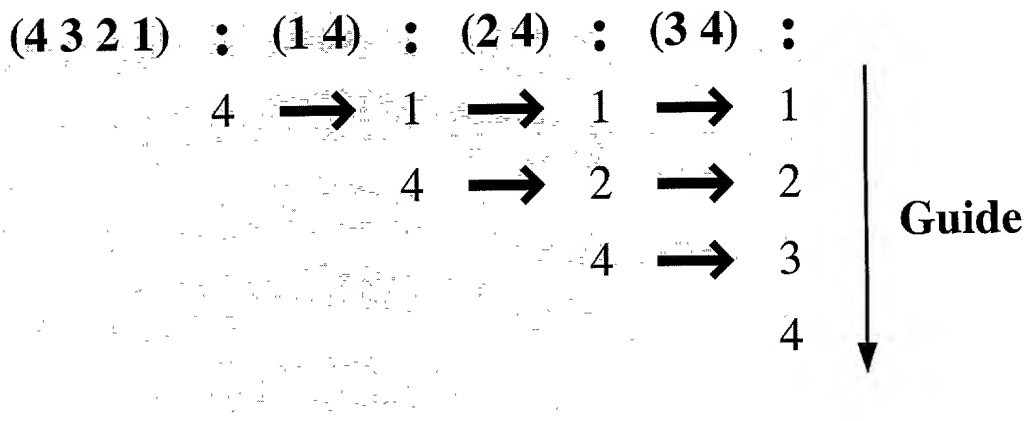



FIG. 28B

PCT/SG2004/000360

FIG. 29

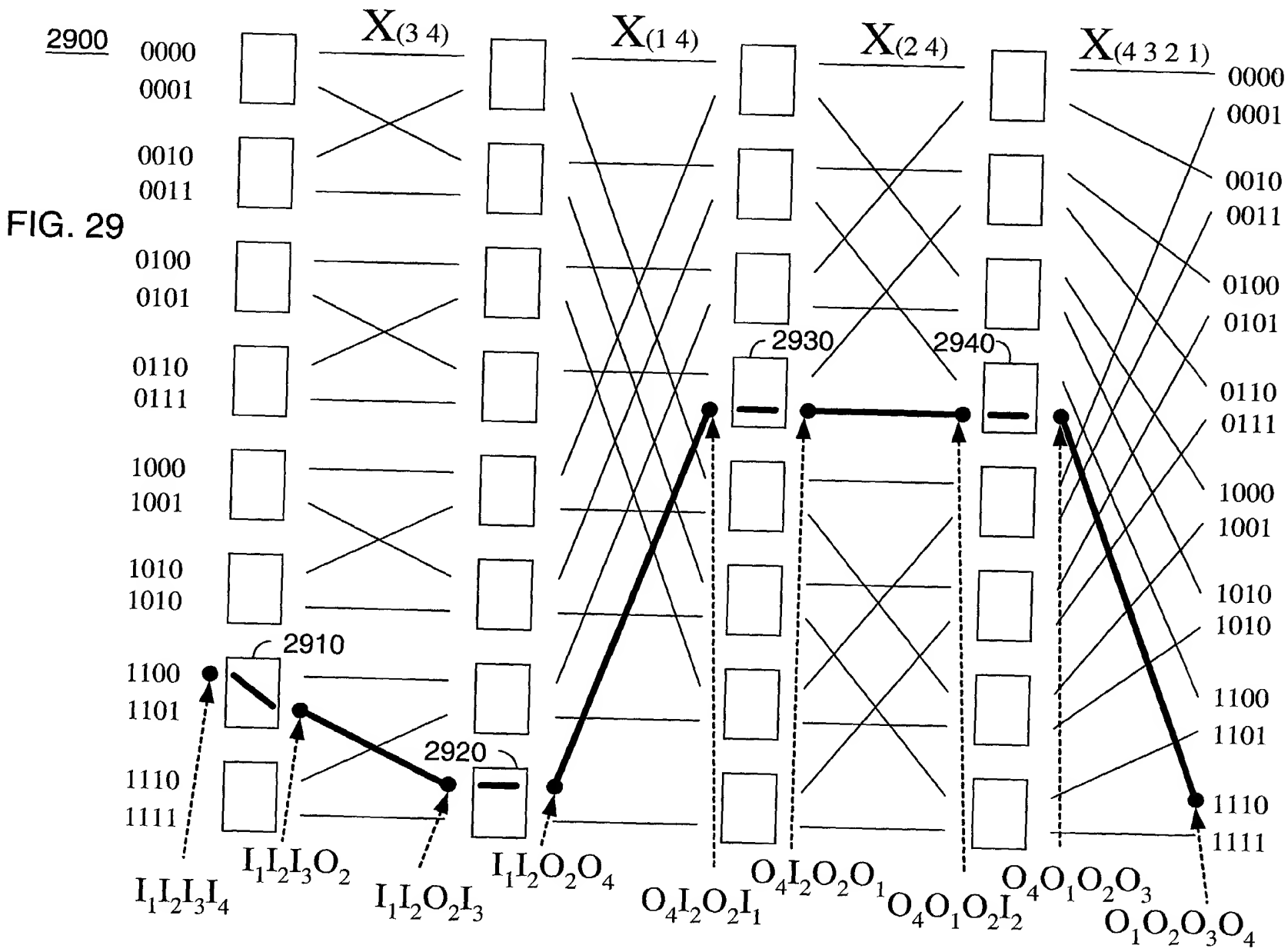


FIG. 30A

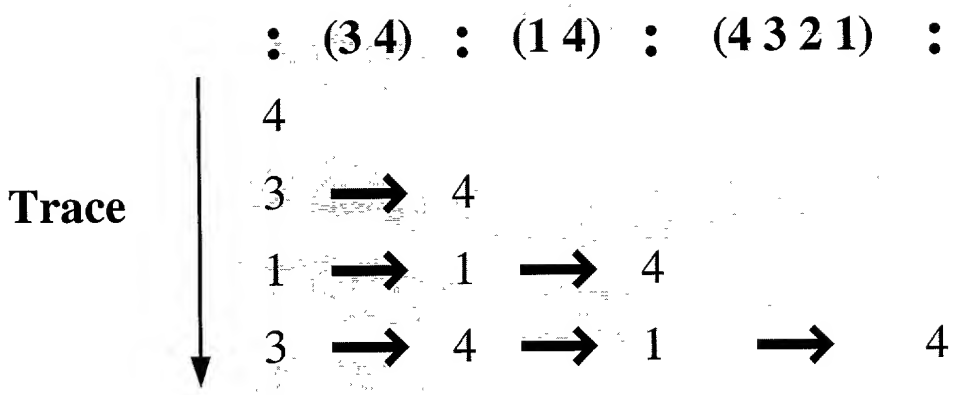
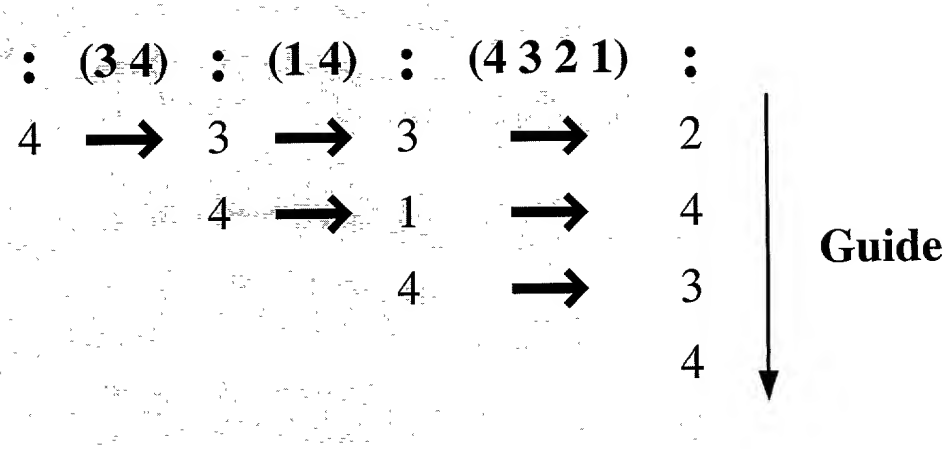



FIG. 30B



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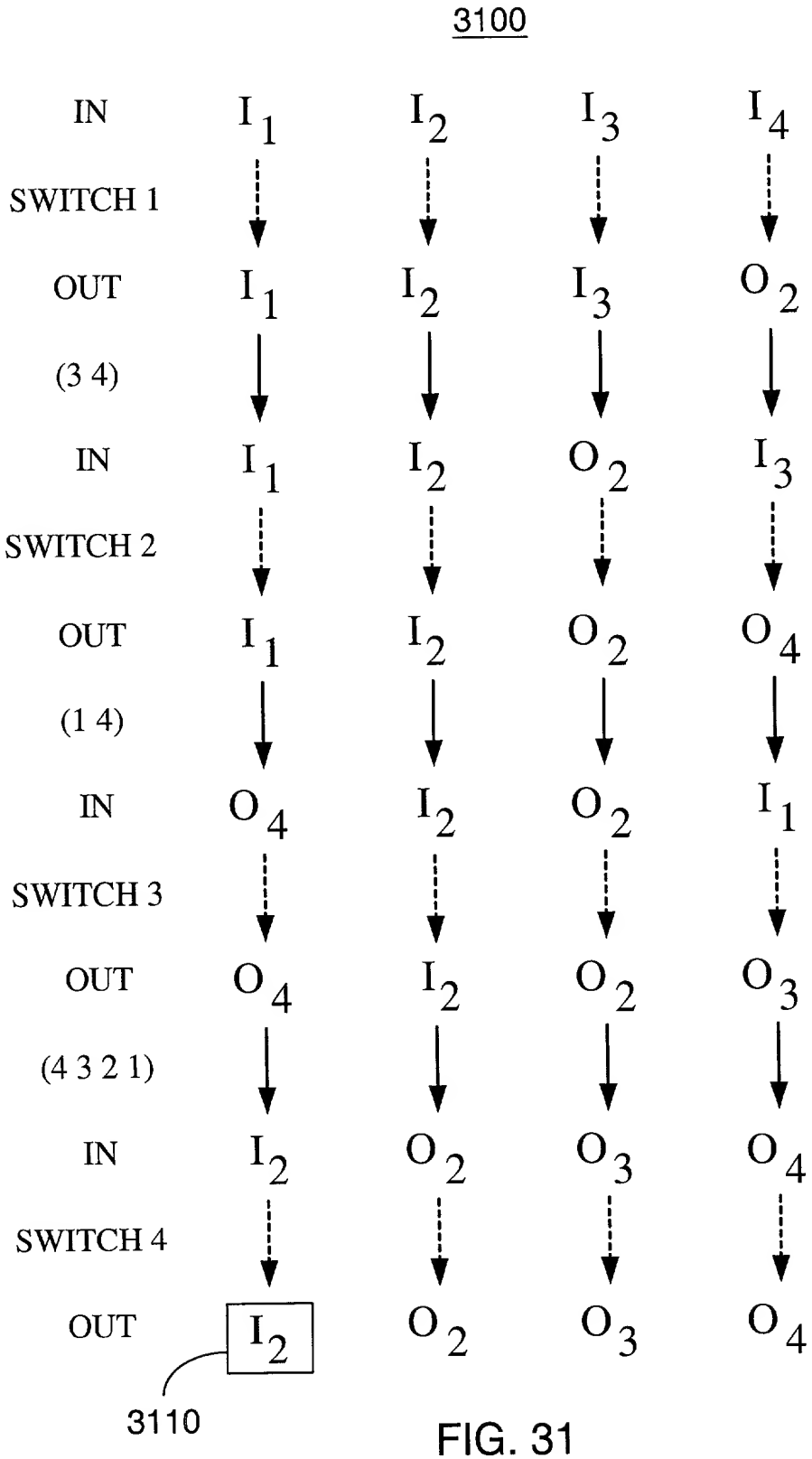


FIG. 31

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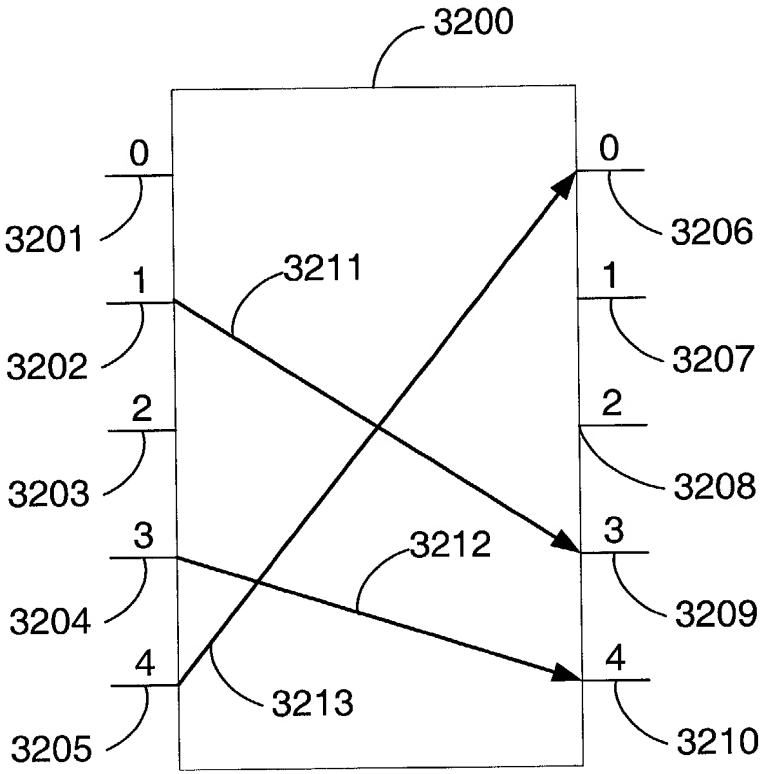


FIG. 32A

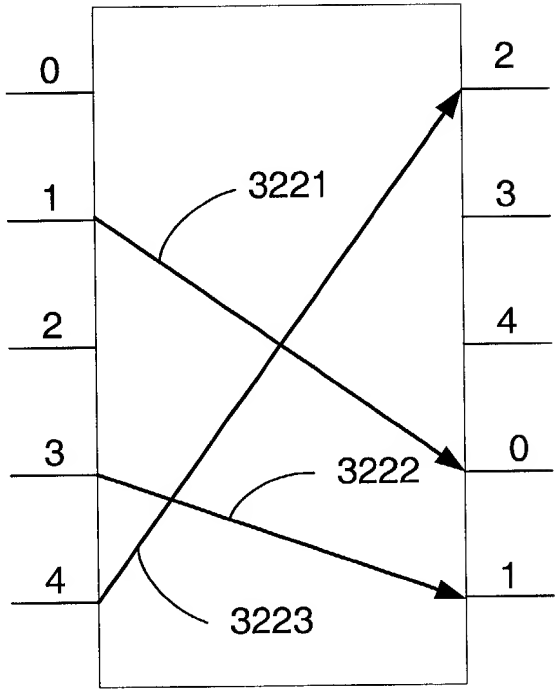


FIG. 32B

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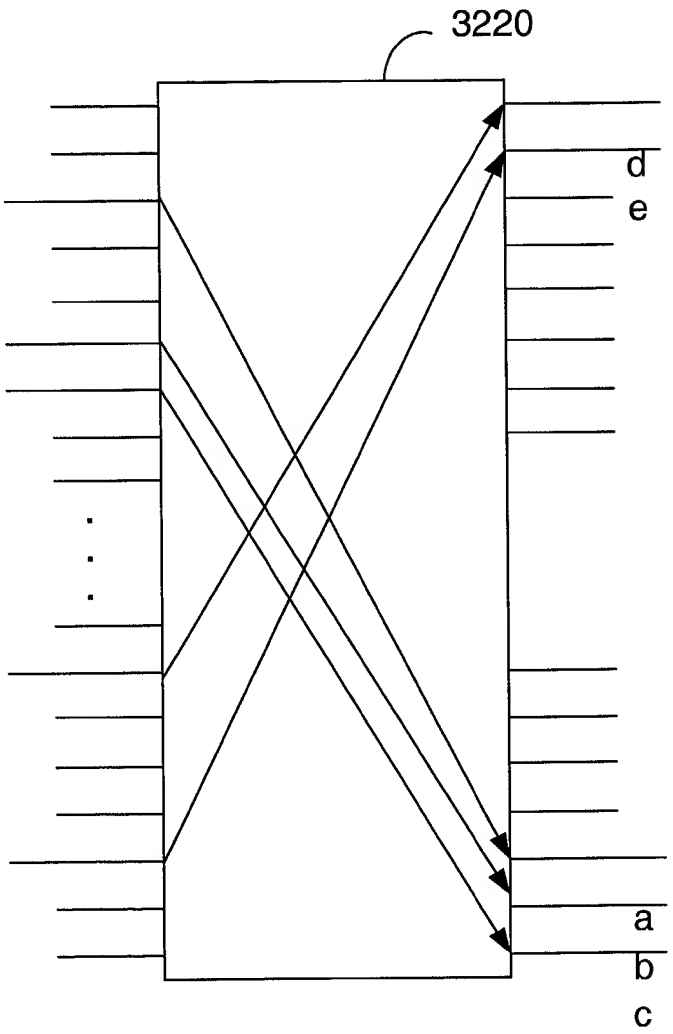


FIG. 32C

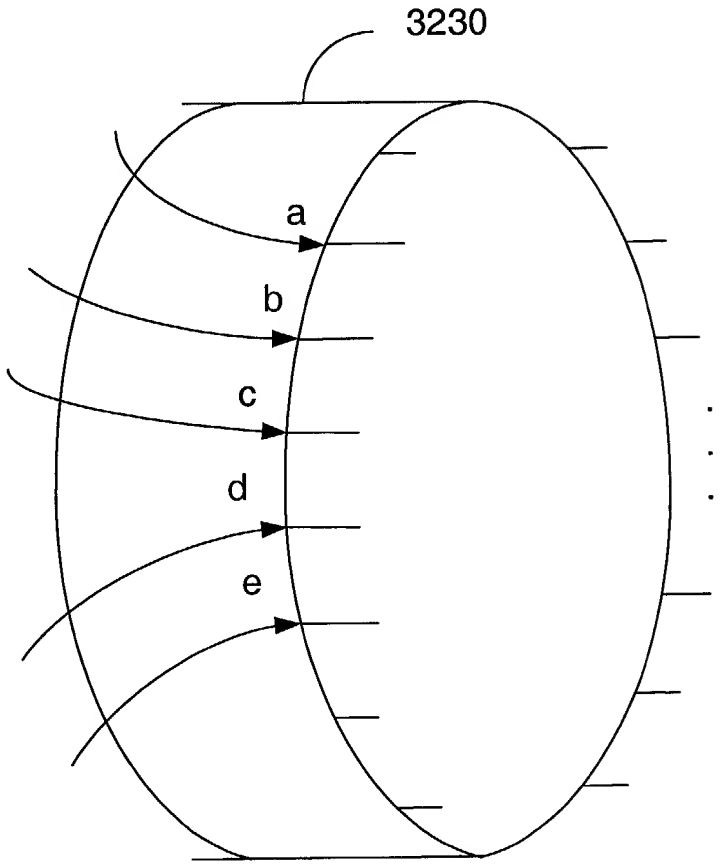


FIG. 32D

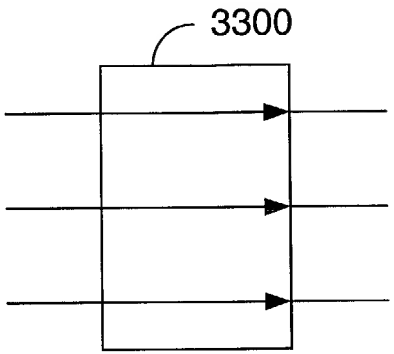


FIG. 33A

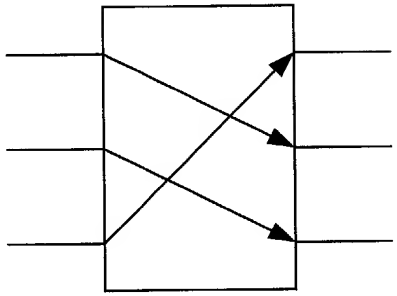

FIG. 33B

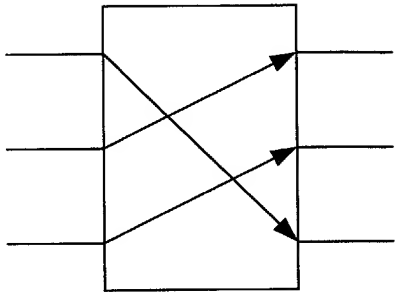

FIG. 33C

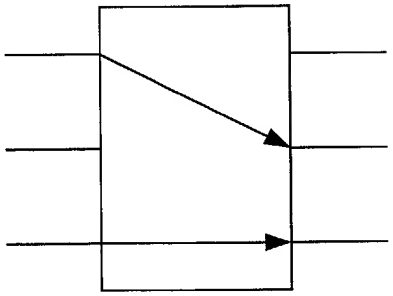

FIG. 33D

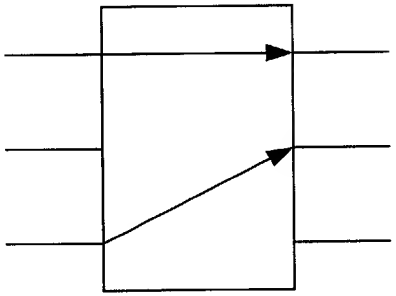

FIG. 33E

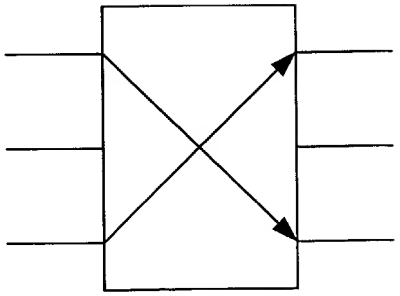

FIG.33F

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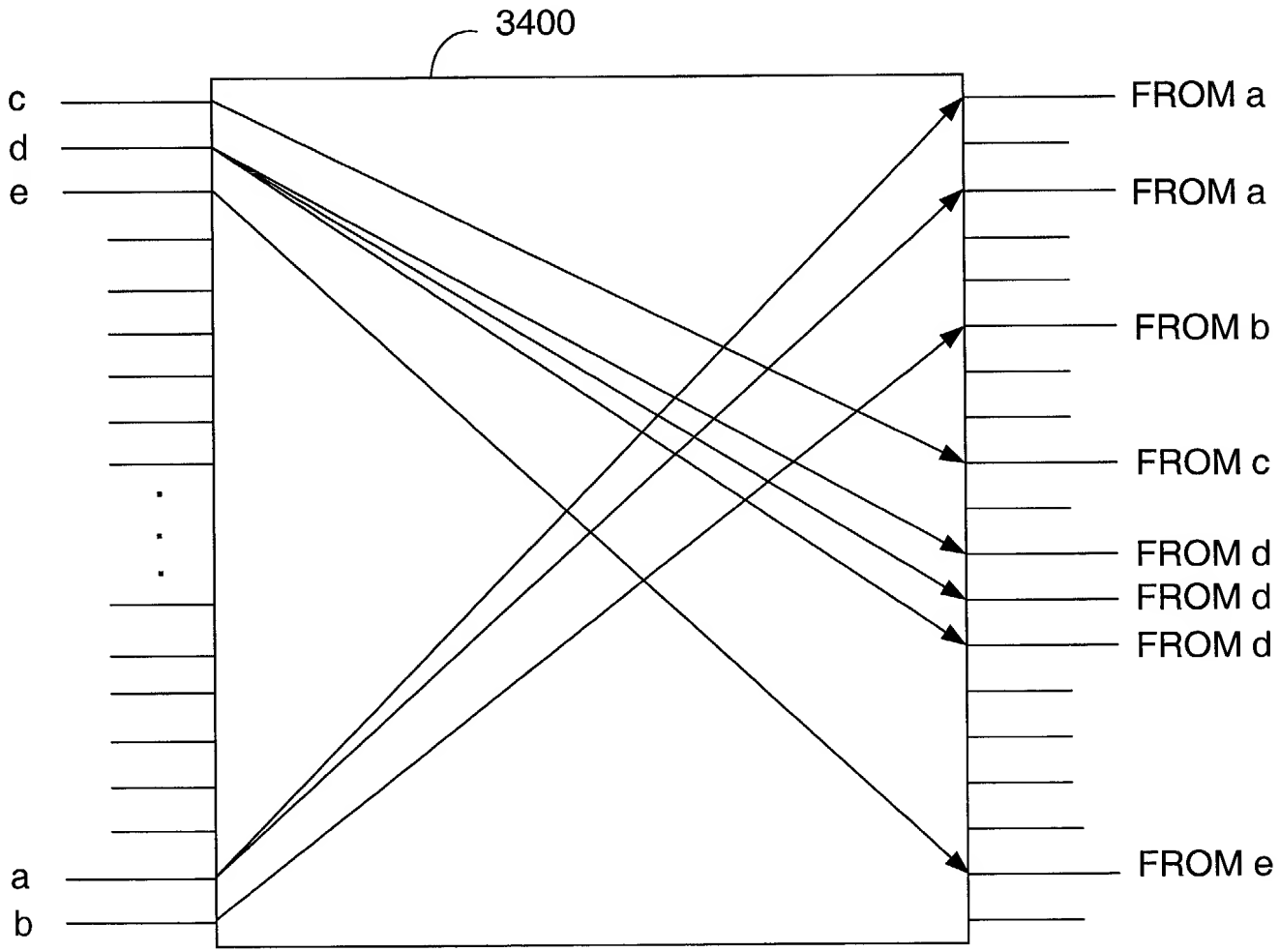



FIG. 34

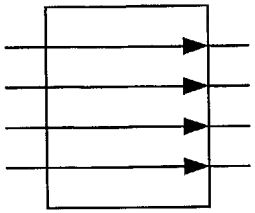


FIG. 35A

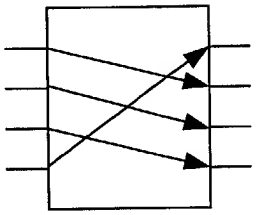


FIG. 35B

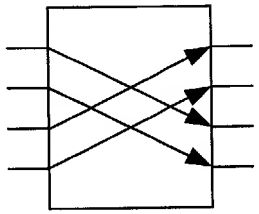


FIG. 35C

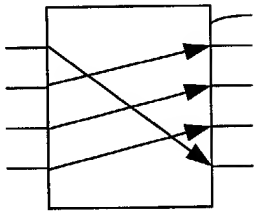



FIG. 35D

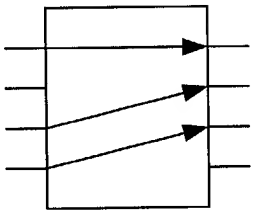


FIG. 35E

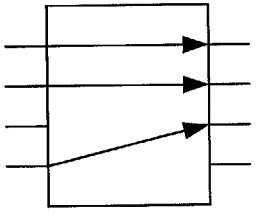


FIG. 35F

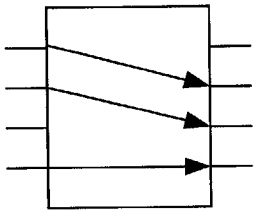


FIG. 35G

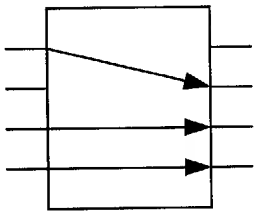


FIG. 35H

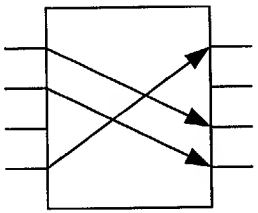


FIG. 35I

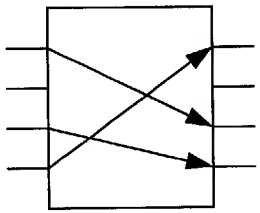


FIG. 35J

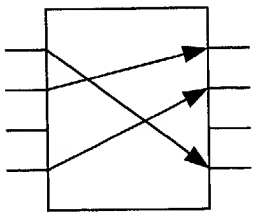


FIG. 35K

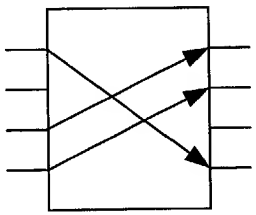


FIG. 35L

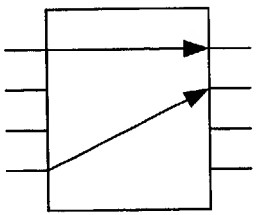


FIG. 35M

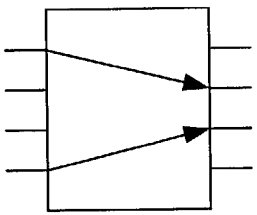


FIG. 35N

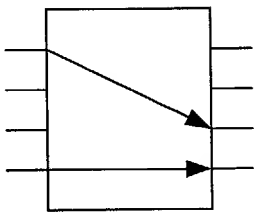


FIG. 35O

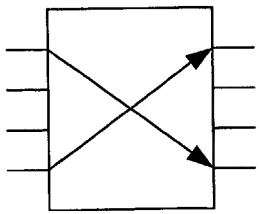


FIG. 35P

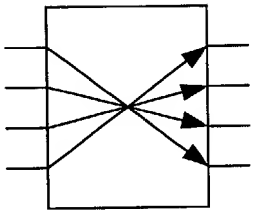


FIG. 36A

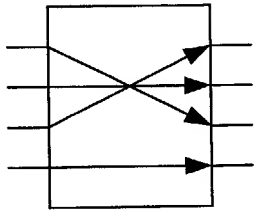


FIG. 36B

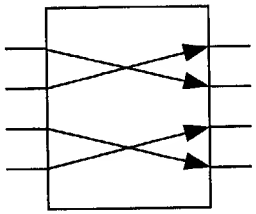


FIG. 36C

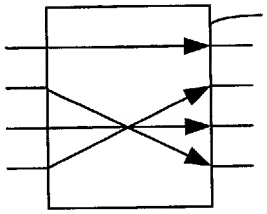



FIG. 36D

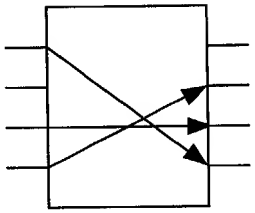


FIG. 36E

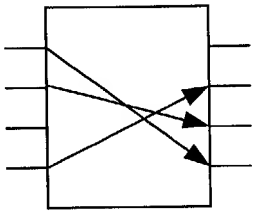


FIG. 36F

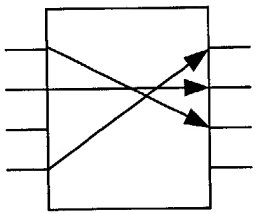


FIG. 36G

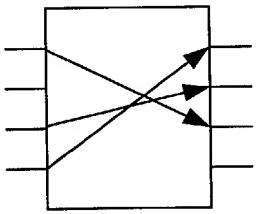


FIG. 36H

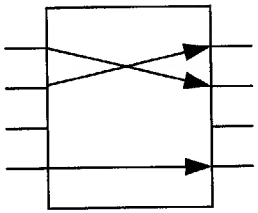


FIG. 36I

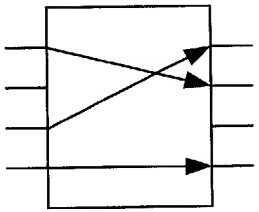


FIG. 36J

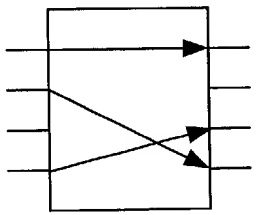


FIG. 36K

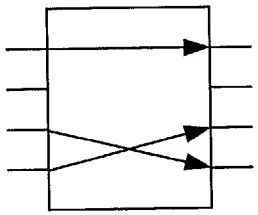


FIG. 36L

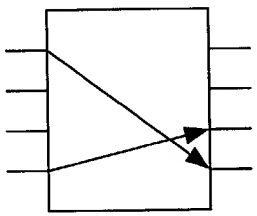


FIG. 36M

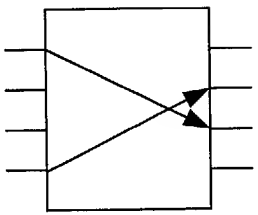


FIG. 36N

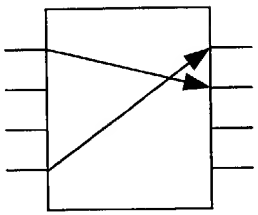


FIG. 36O

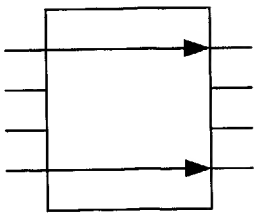


FIG. 36P

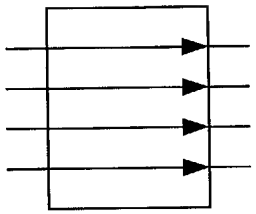


FIG. 37A

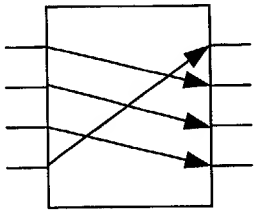


FIG. 37B

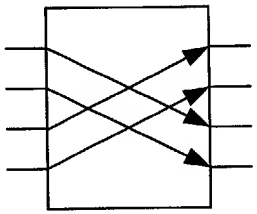


FIG. 37C

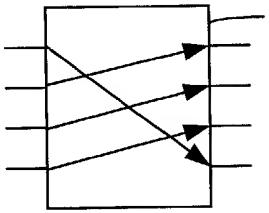



FIG. 37D

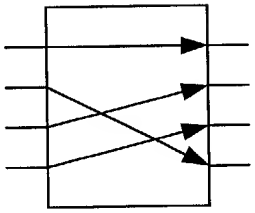


FIG. 37E

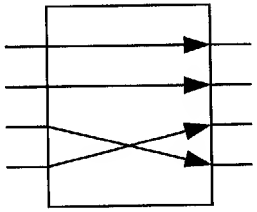


FIG. 37F

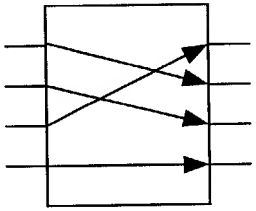


FIG. 37G

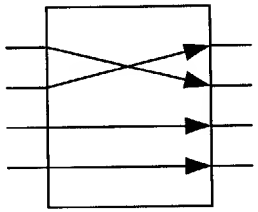


FIG. 37H

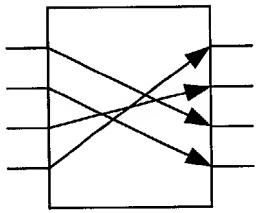


FIG. 37I

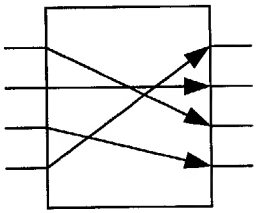


FIG. 37J

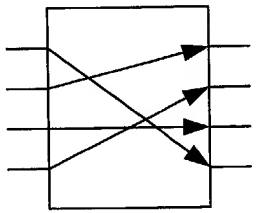


FIG. 37K

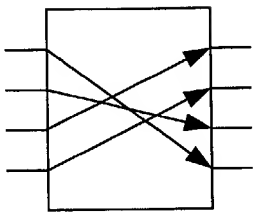


FIG. 37L

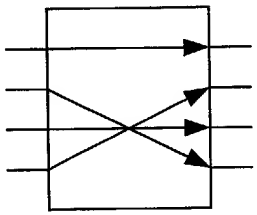


FIG. 37M

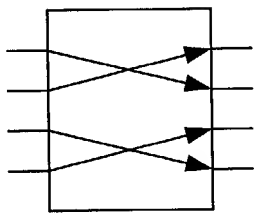


FIG. 37N

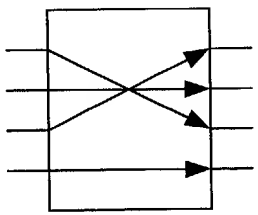


FIG. 37O

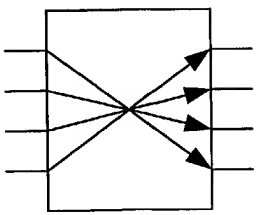
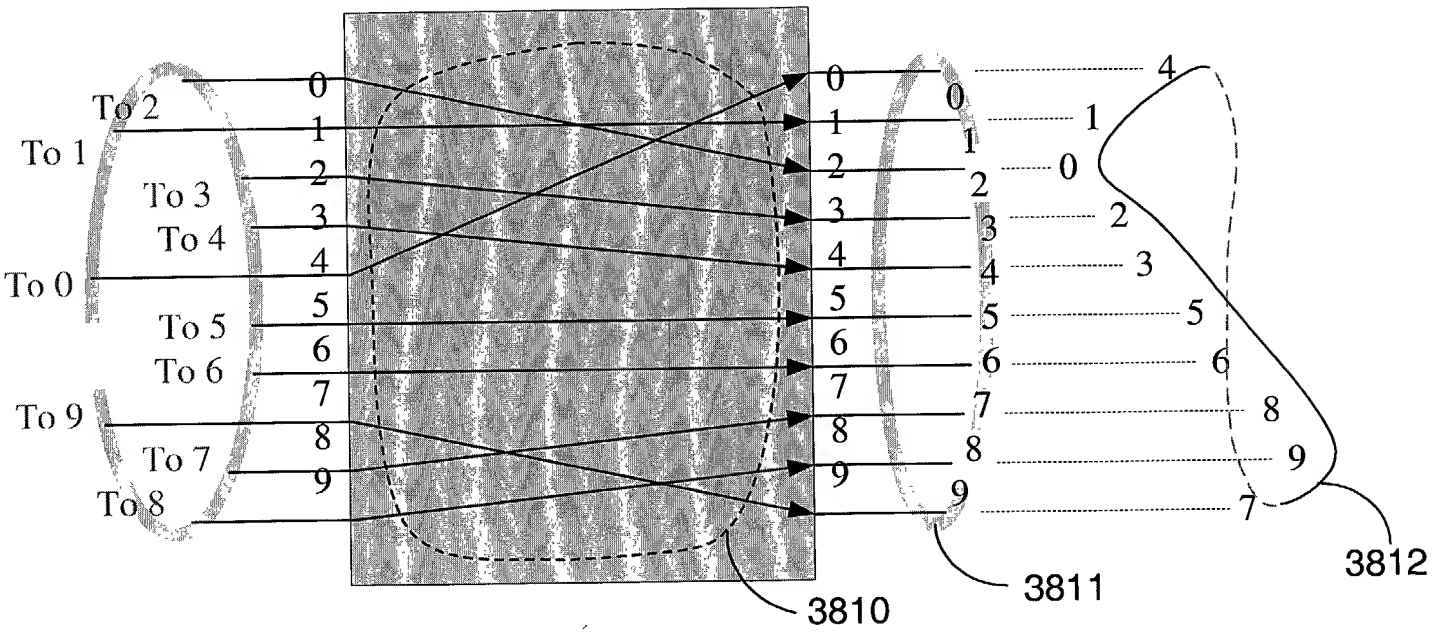


FIG. 37P


To 2
To 1
To 3
To 4
To 0
To 5
To 6
To 9
To 7
To 8
0
1
2
3
4
5
6
7
8
9
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6
7
8
9
0
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5
6
7
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9
4
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0
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6
8
9
7
3810
3811
3812

FIG. 38A

TOP SECRET

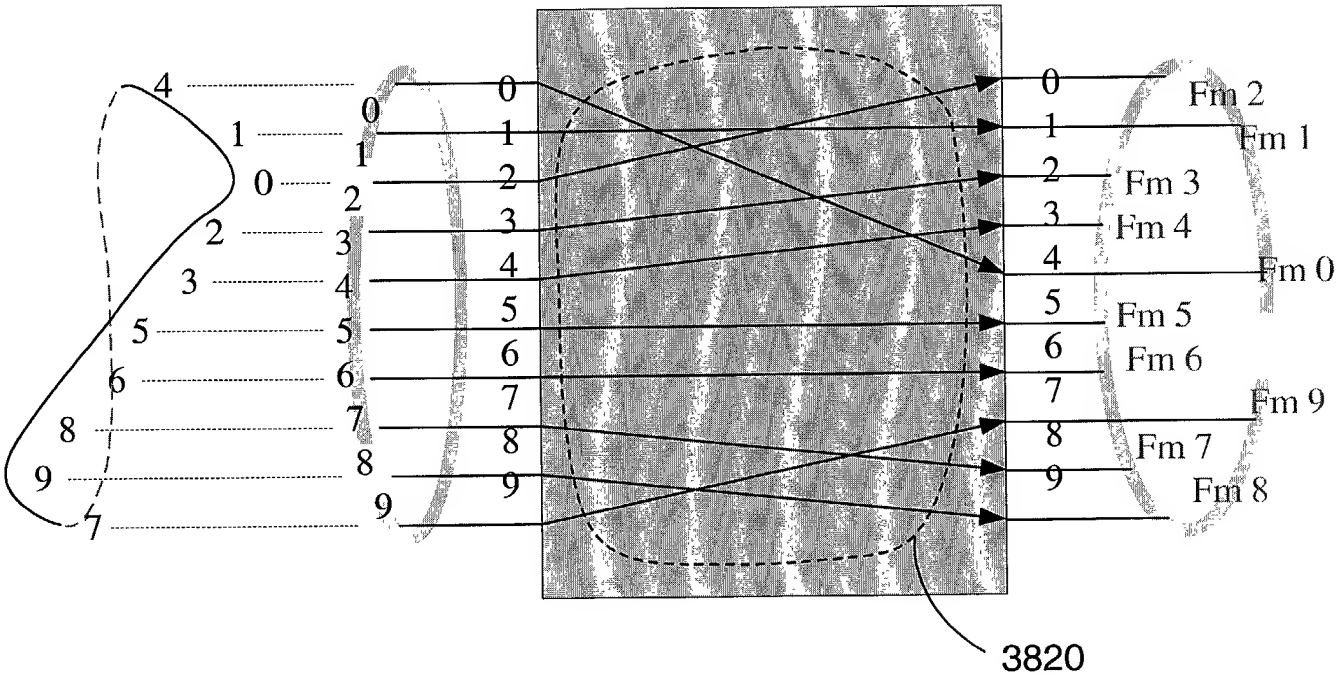


FIG.38B

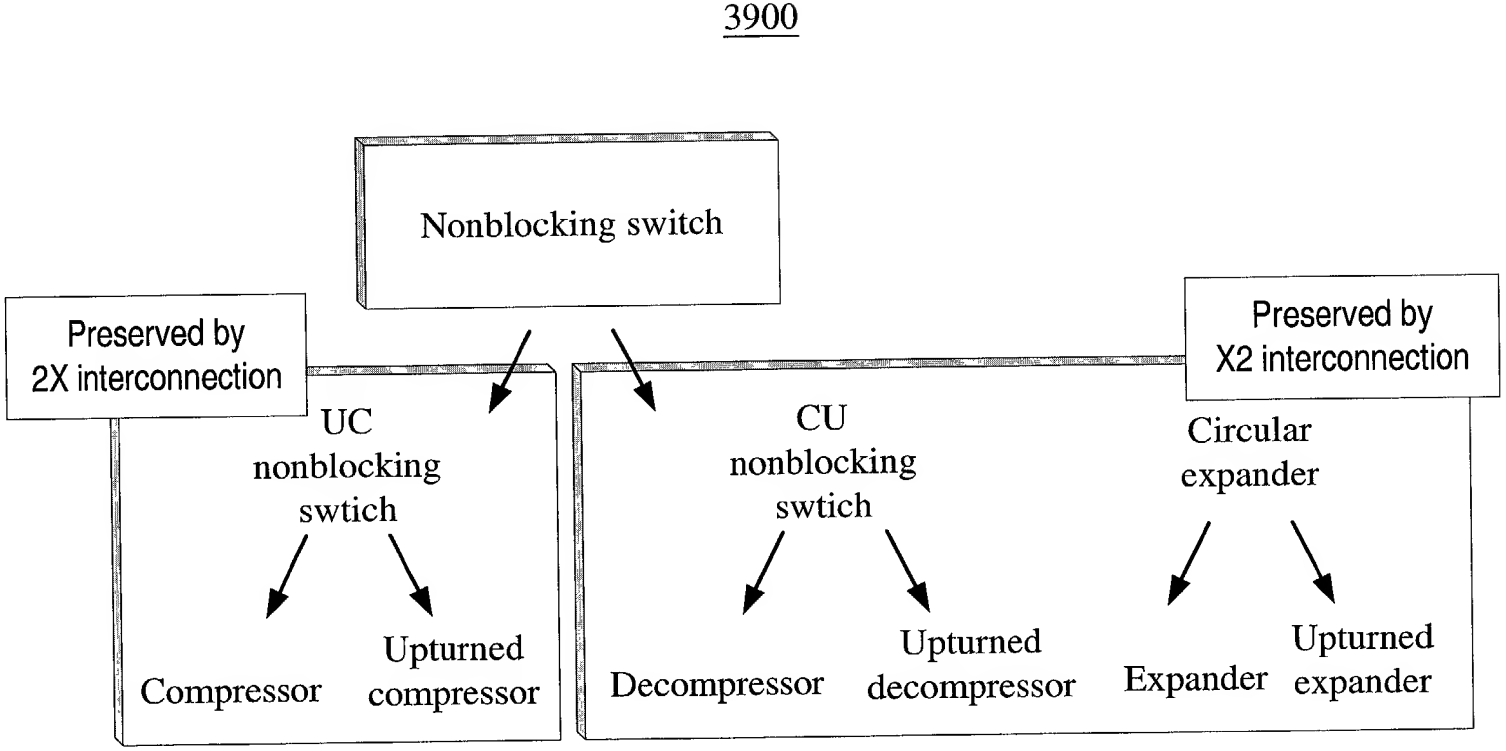
3900
Nonblocking switch
Preserved by
2X interconnection
Preserved by
X2 interconnection
UC
nonblocking
swtich
CU
nonblocking
swtich
Circular
expander
Compressor
Upturned
compressor
Decompressor
Upturned
decompressor
Expander
Upturned
expander

FIG. 39

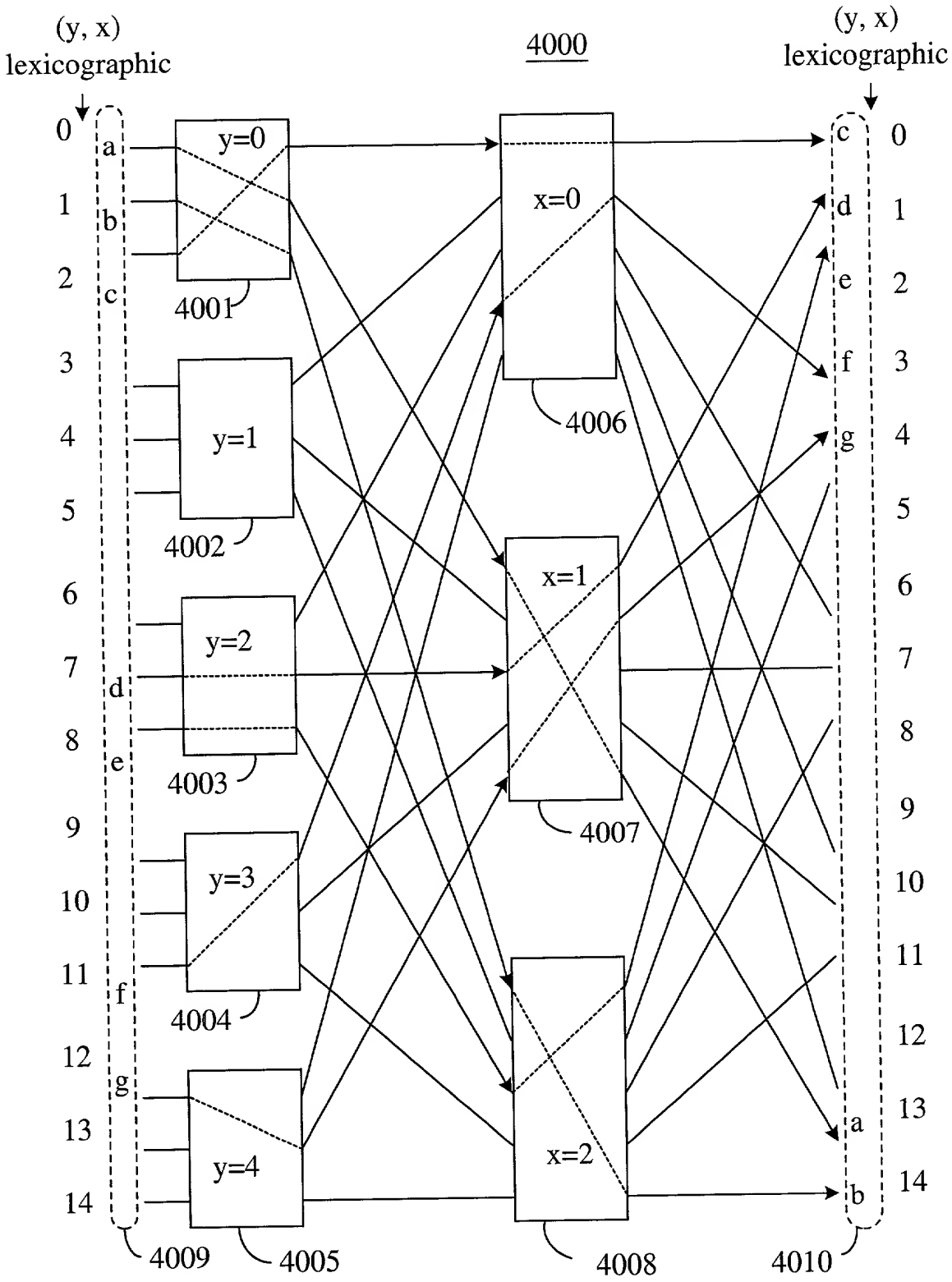
(y, x)
lexicographic
4000
(y, x)
lexicographic
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
a
b
c
d
e
f
g
y=0
y=1
y=2
y=3
y=4
x=0
x=1
x=2
4001
4002
4003
4004
4005
4006
4007
4008
4009
4010

FIG. 40

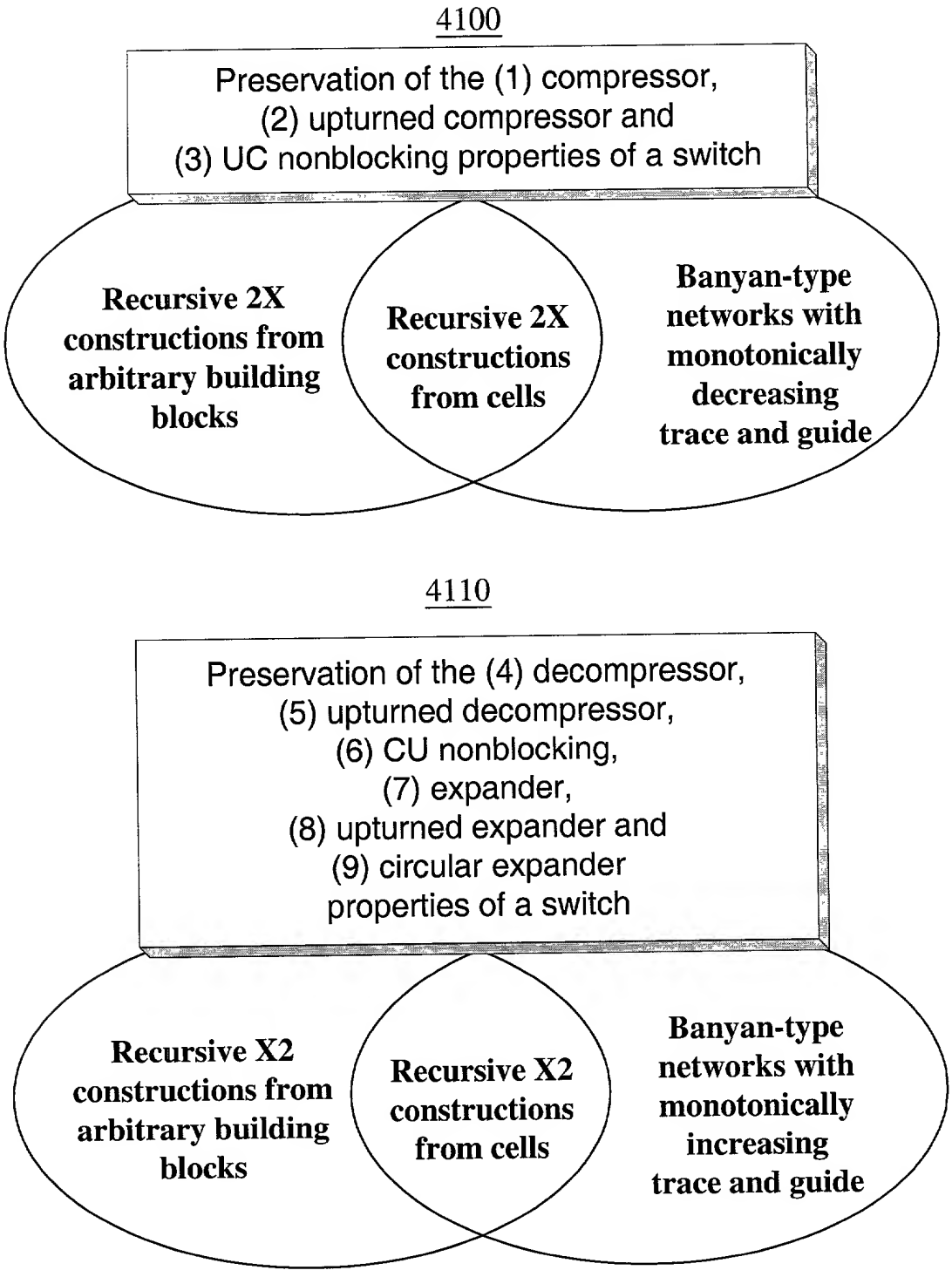
4100
Preservation of the (1) compressor,
(2) upturned compressor and
(3) UC nonblocking properties of a switch
Recursive 2X constructions from arbitrary building blocks
Recursive 2X constructions from cells
Banyan-type networks with monotonically decreasing trace and guide
4110
Preservation of the (4) decompressor,
(5) upturned decompressor,
(6) CU nonblocking,
(7) expander,
(8) upturned expander and
(9) circular expander
properties of a switch
Recursive X2 constructions from arbitrary building blocks
Recursive X2 constructions from cells
Banyan-type networks with monotonically increasing trace and guide

FIG. 41

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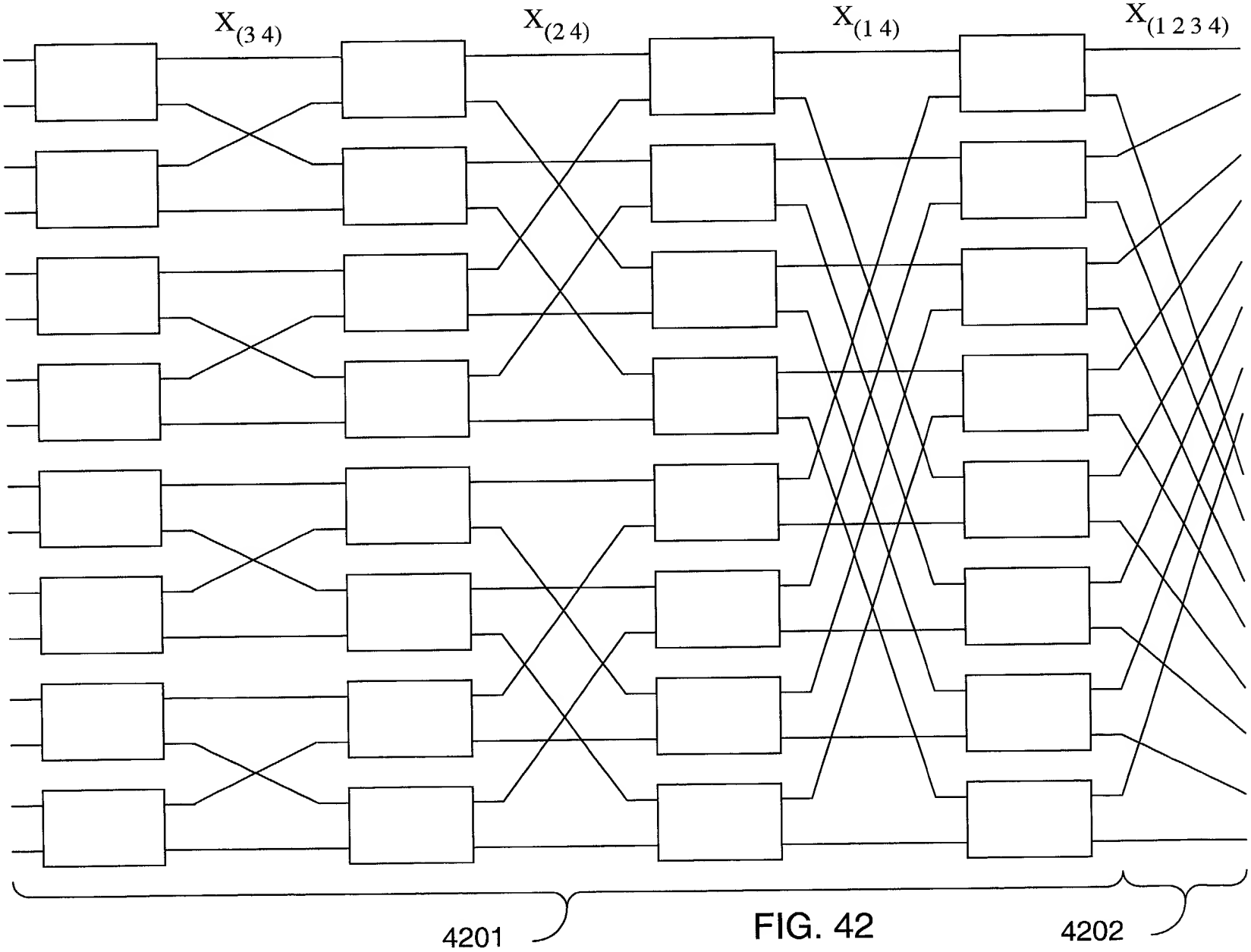



FIG. 42

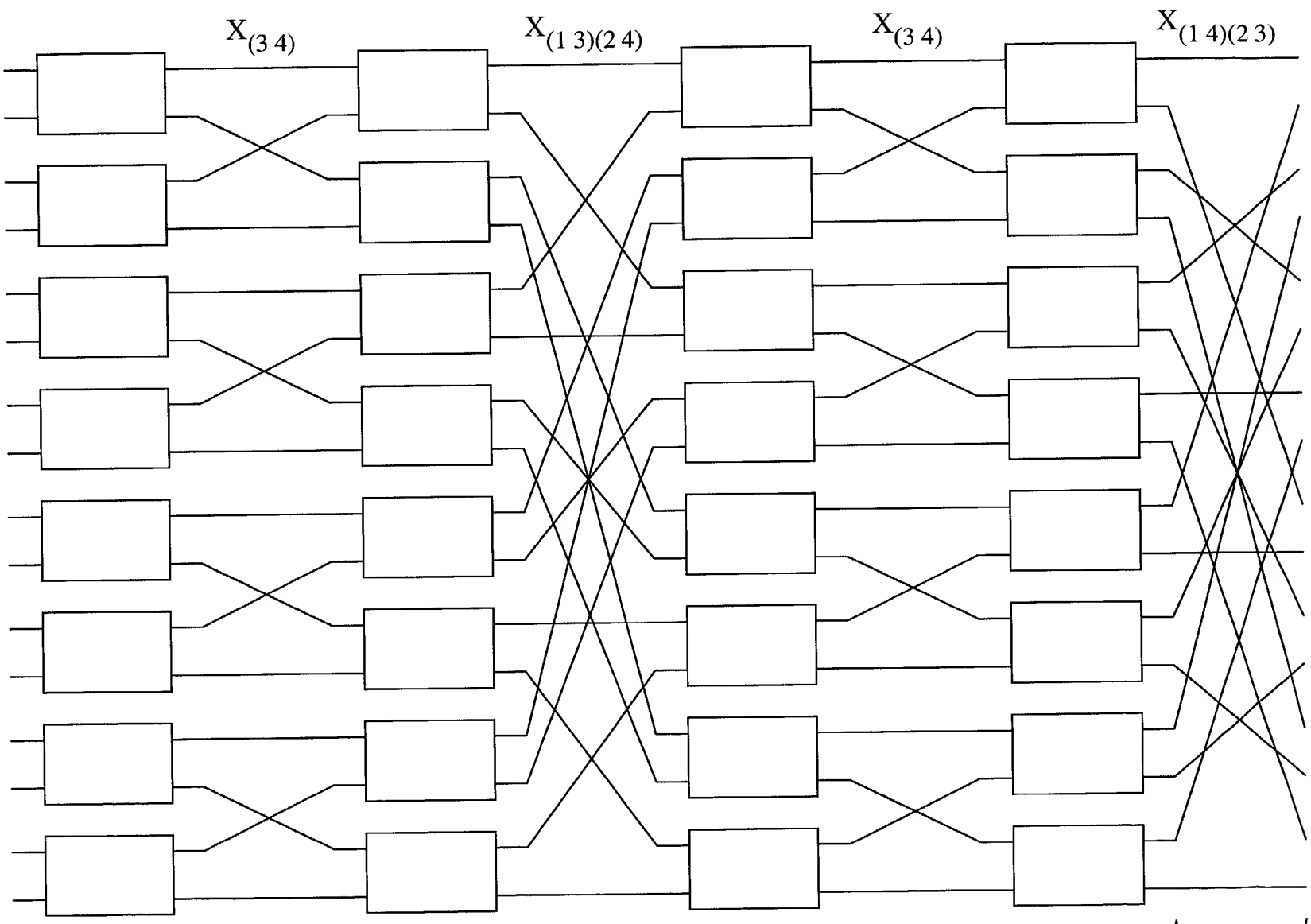



FIG. 43

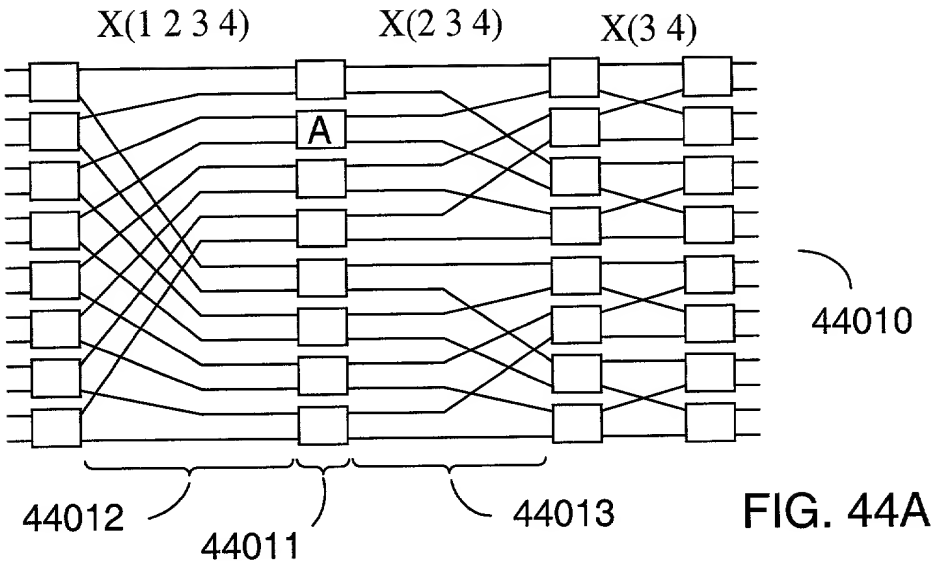



FIG. 44A

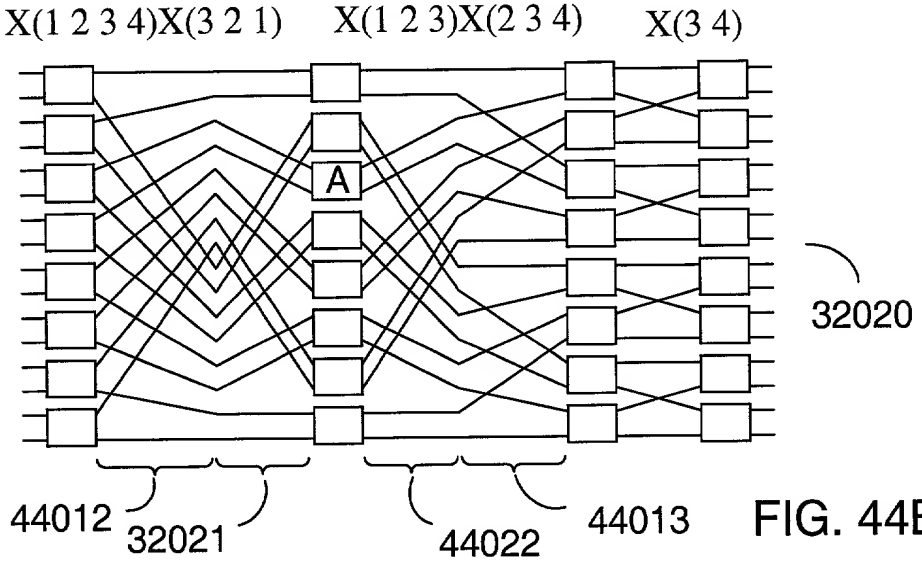



FIG. 44B

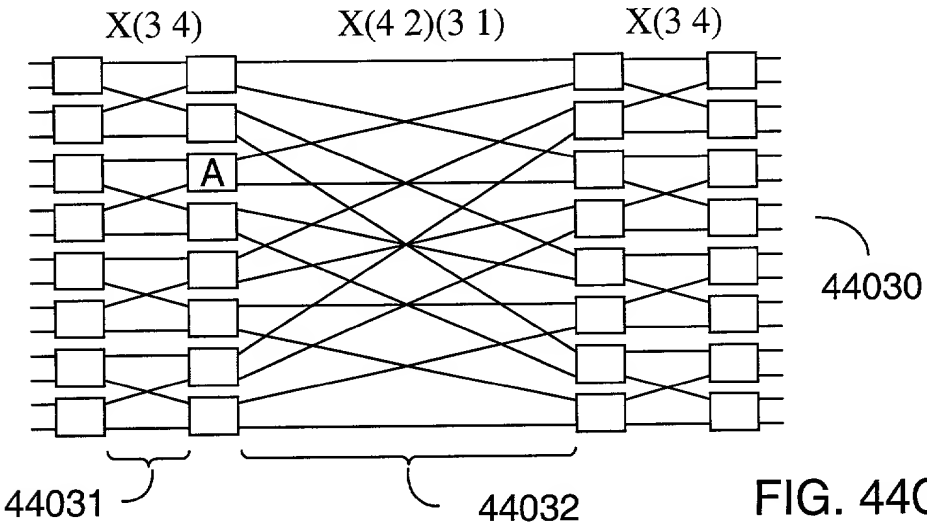



FIG. 44C

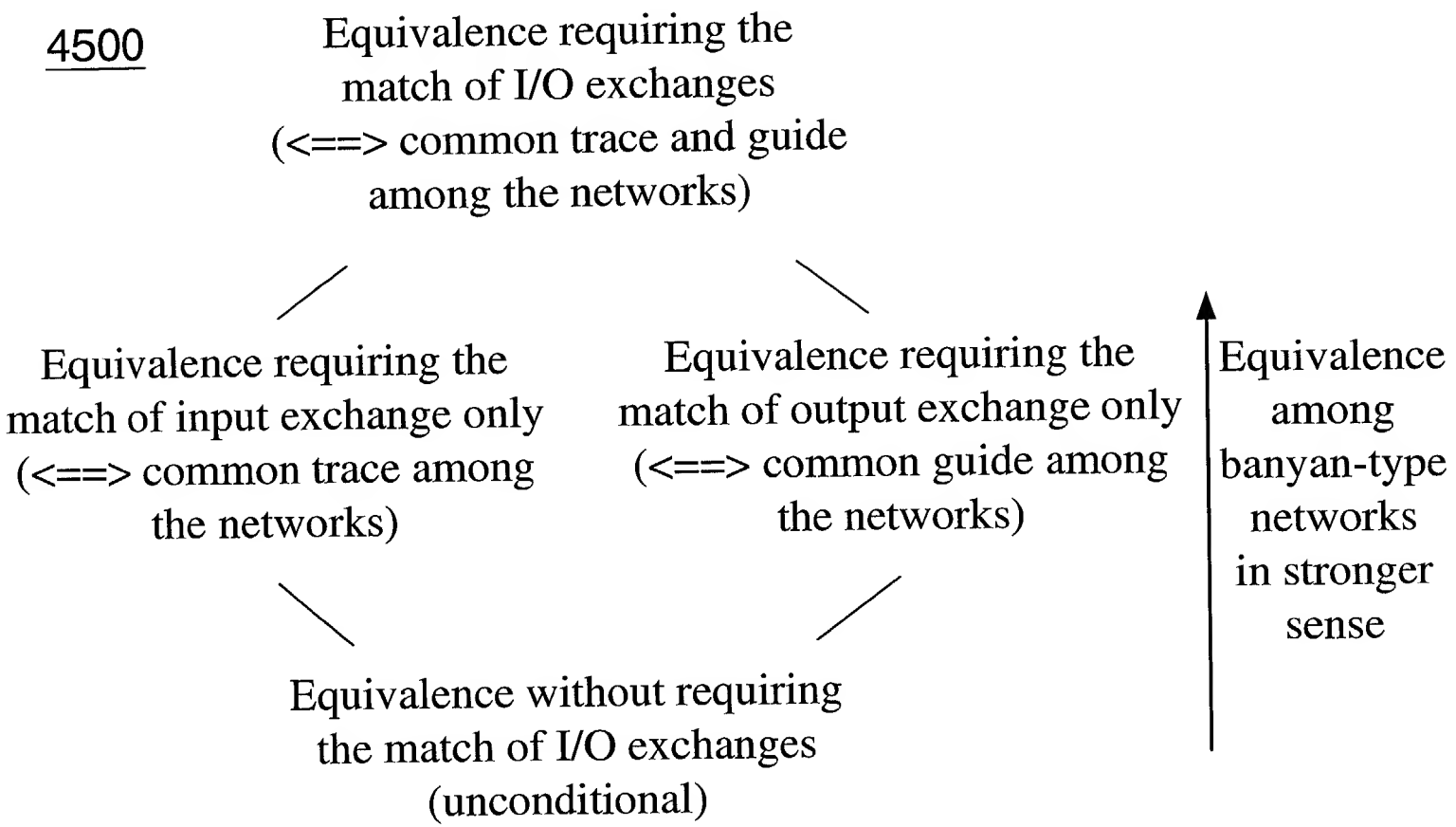

4500
Equivalence requiring the match of I/O exchanges (<==> common trace and guide among the networks)
Equivalence requiring the match of input exchange only (<==> common trace among the networks)
Equivalence requiring the match of output exchange only (<==> common guide among the networks)
Equivalence without requiring the match of I/O exchanges (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 45

PCT/JP2004/018010

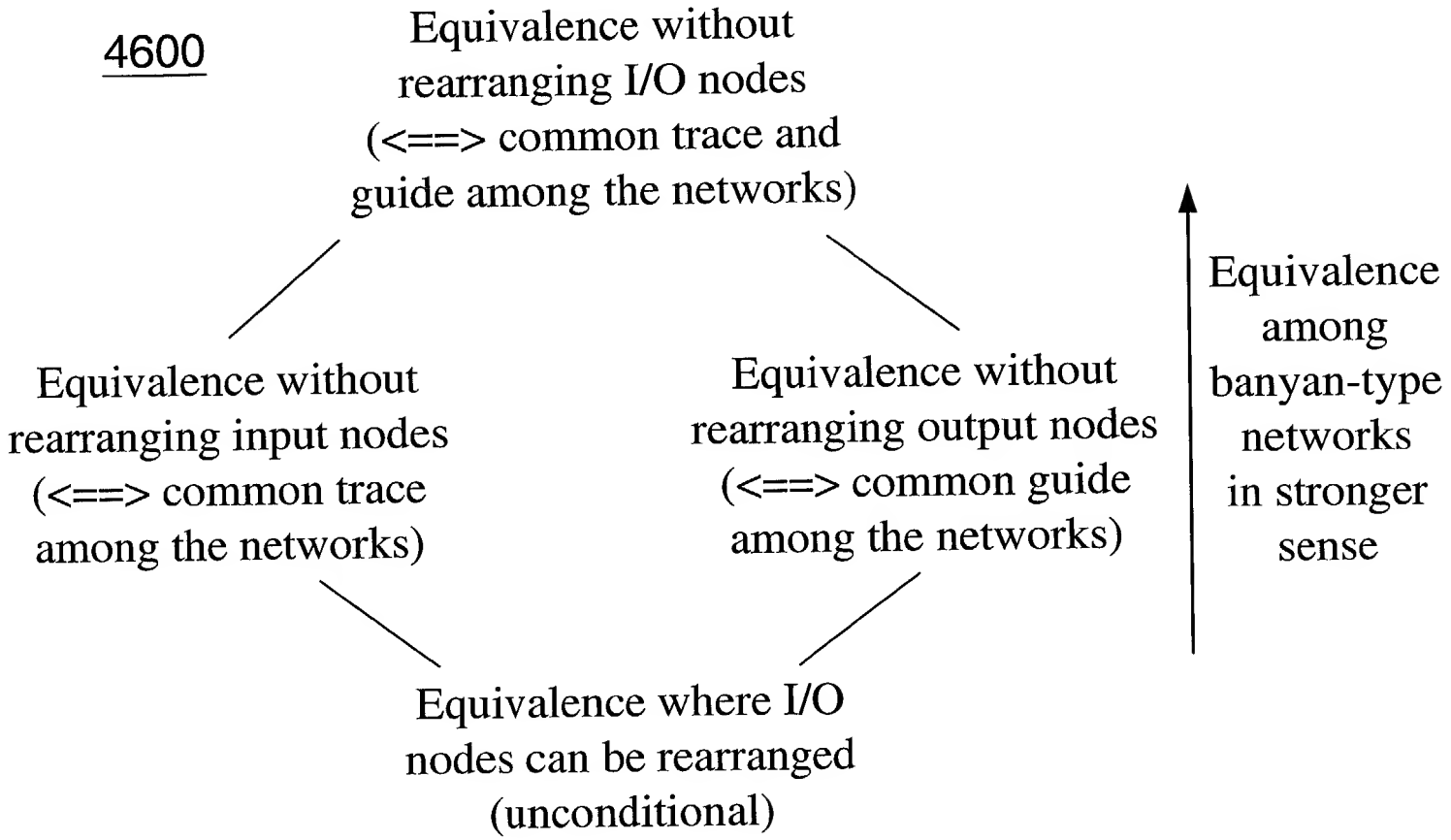



**FIG. 46**

Patent Application

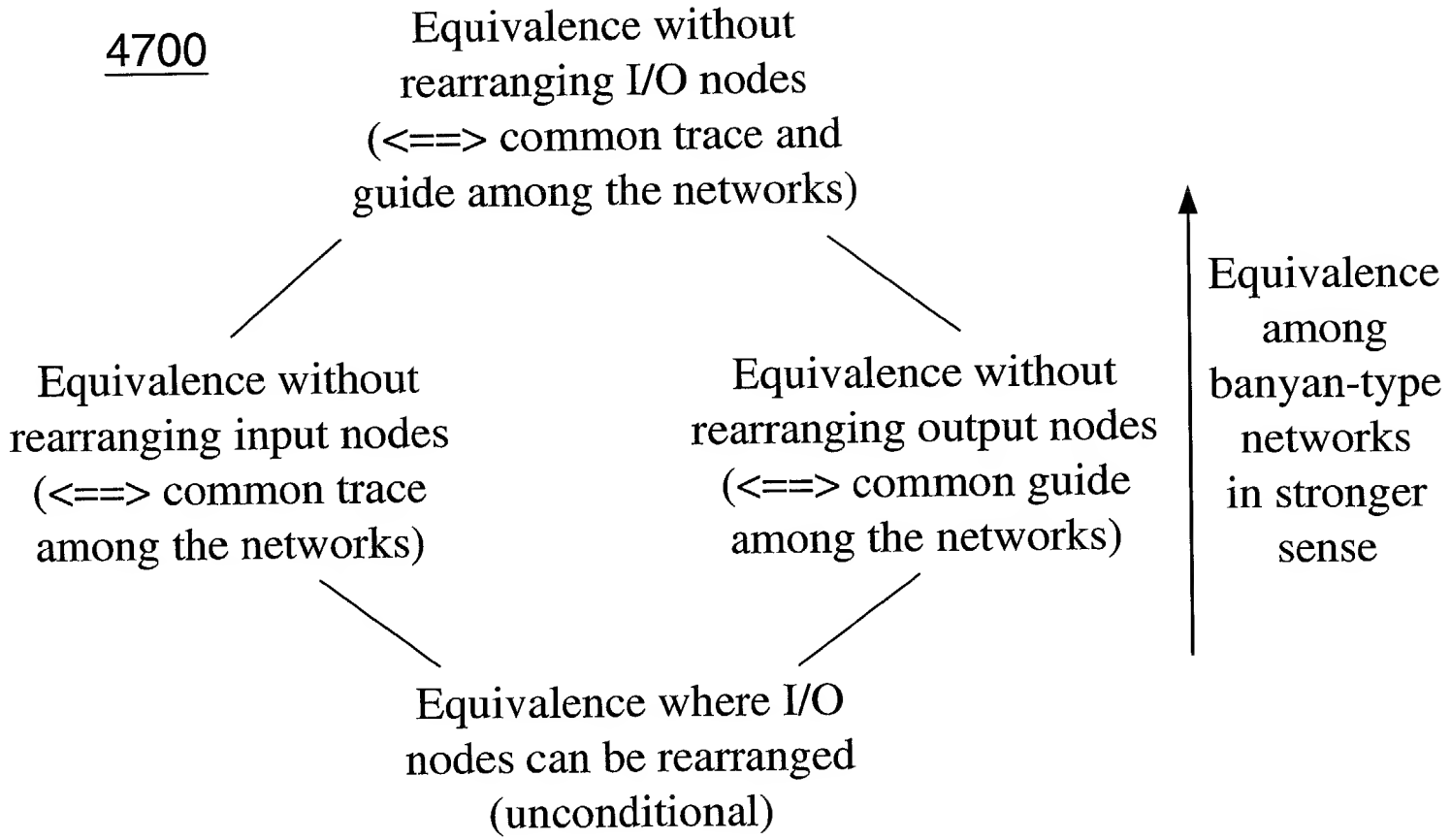



**FIG. 47**

TOSHIBA 2001P0805

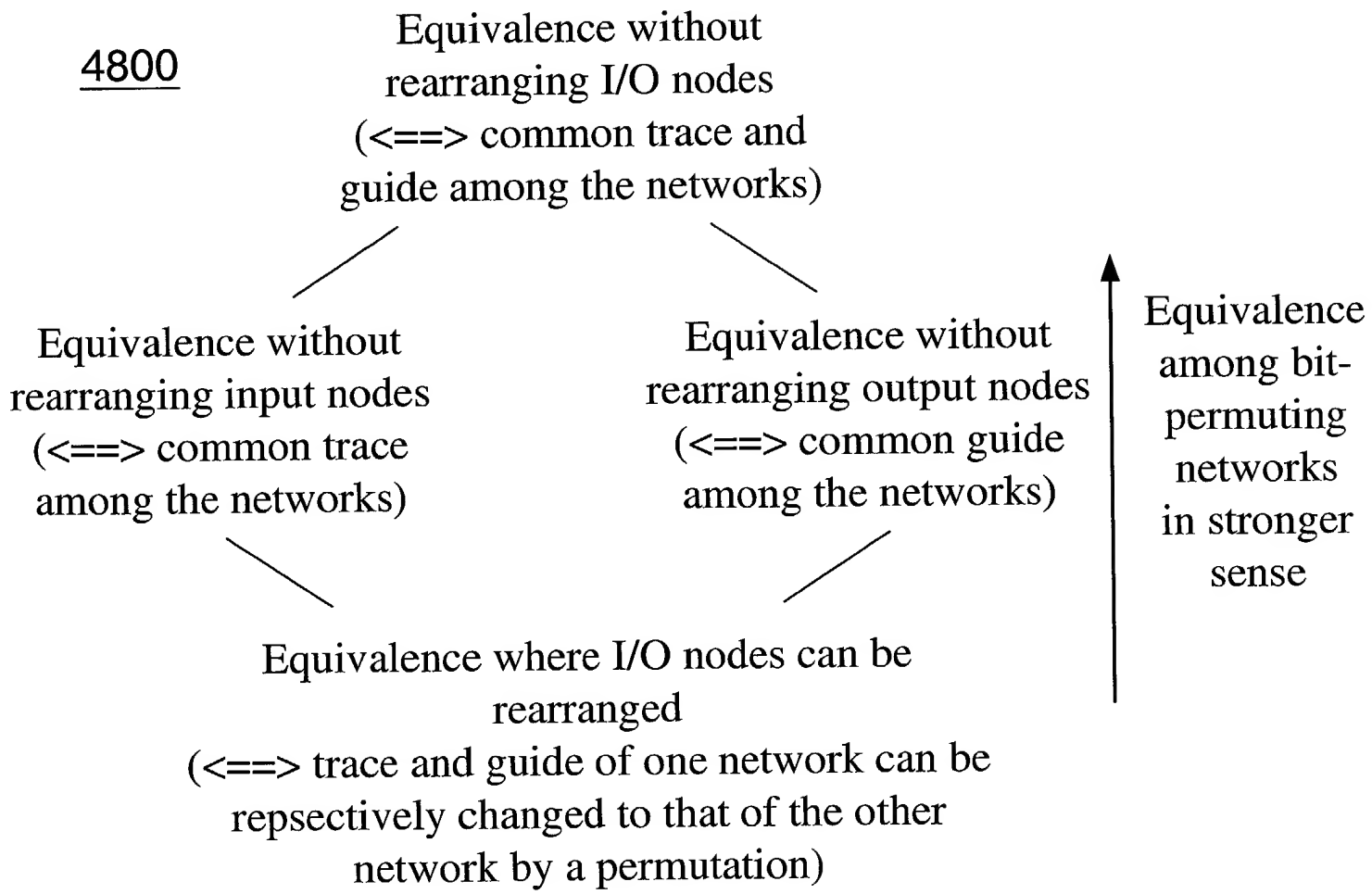



**FIG. 48**

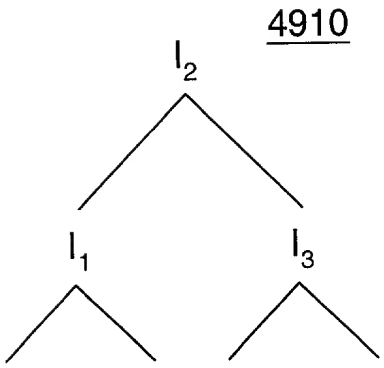



FIG. 49A

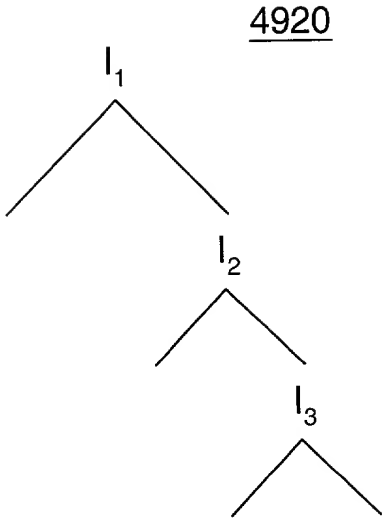



FIG. 49B

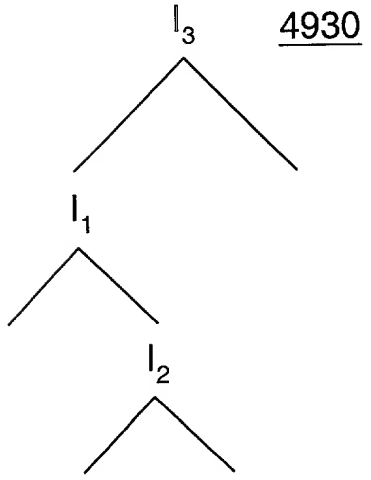



FIG. 49C

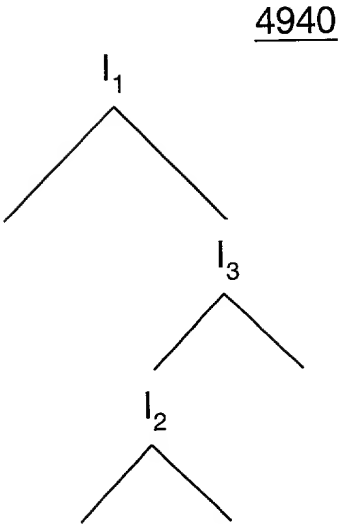



FIG. 49D

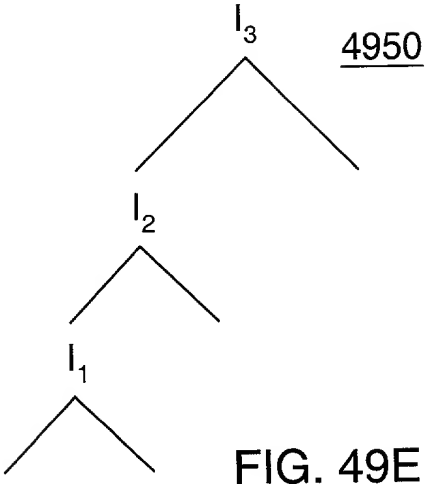



FIG. 49E

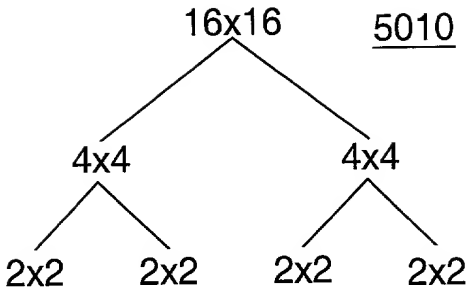



FIG. 50A

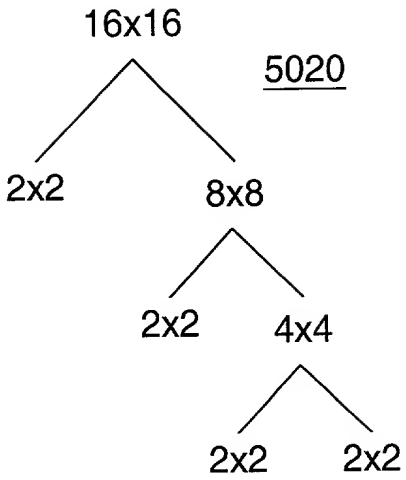



FIG. 50B

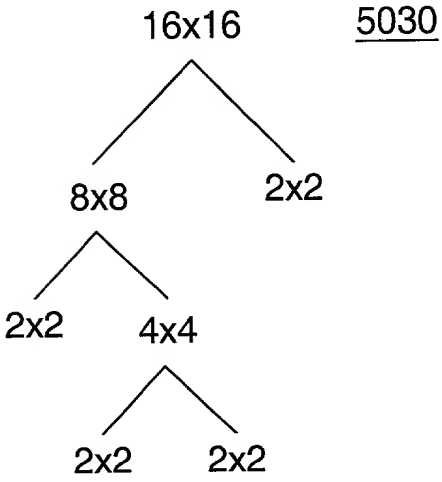



FIG. 50C

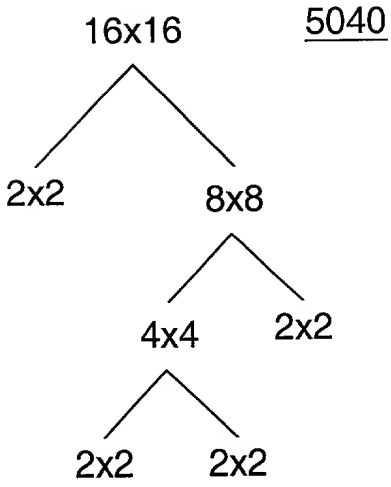



FIG. 50D

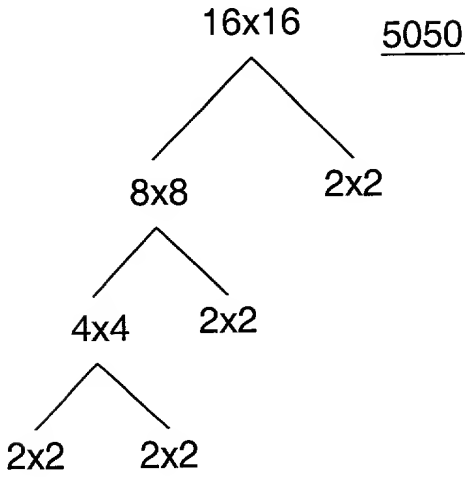



FIG. 50E

5100

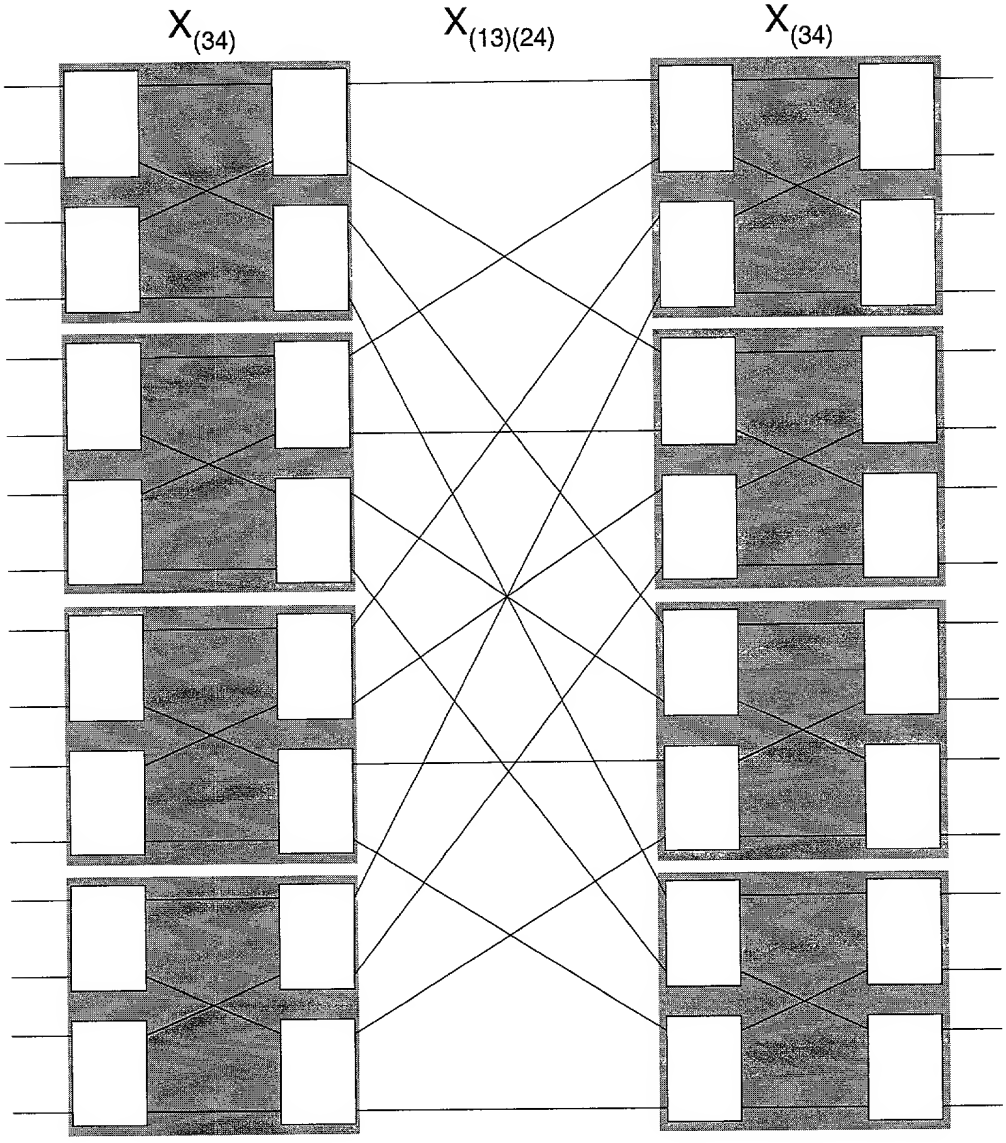



FIG. 51

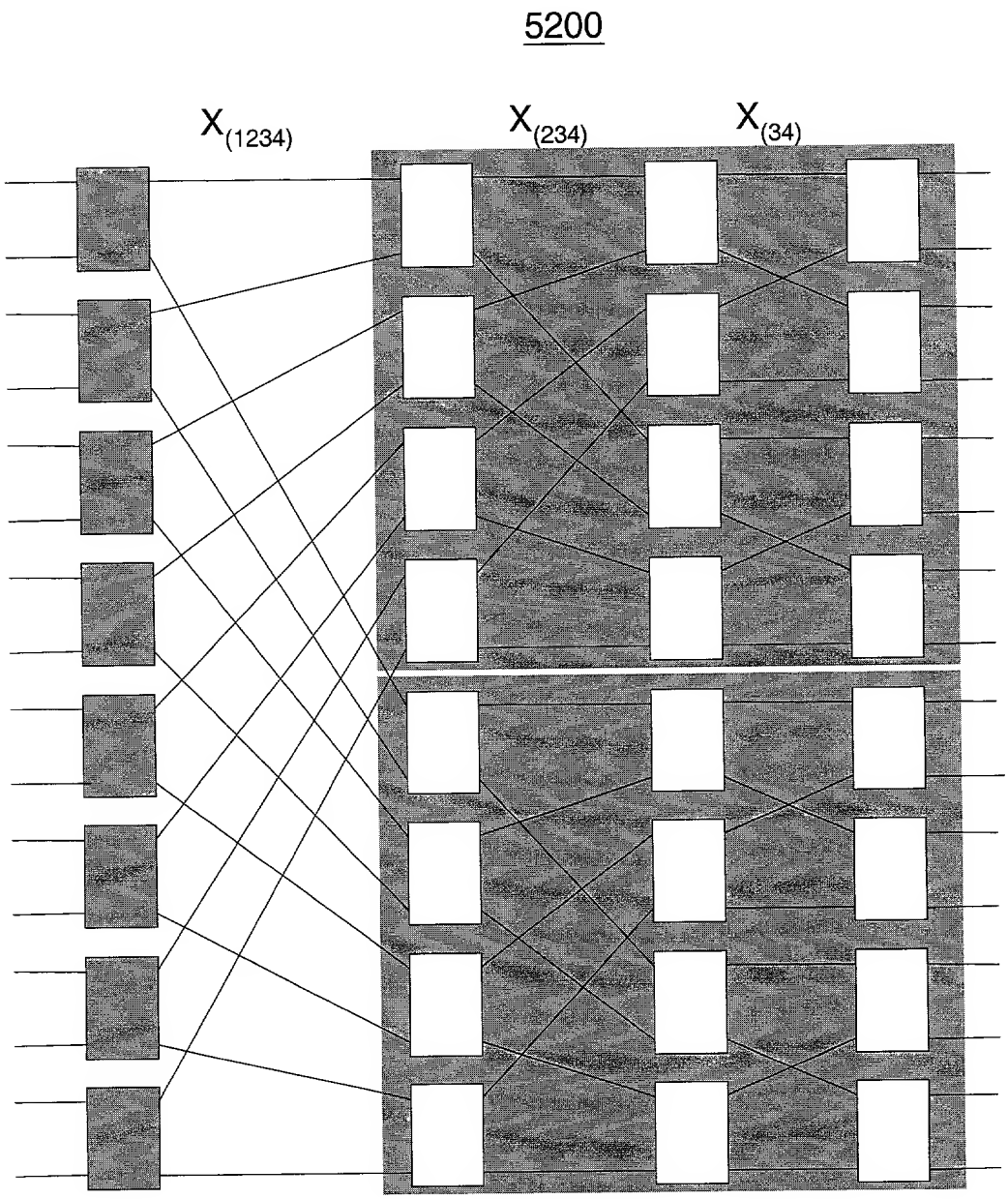
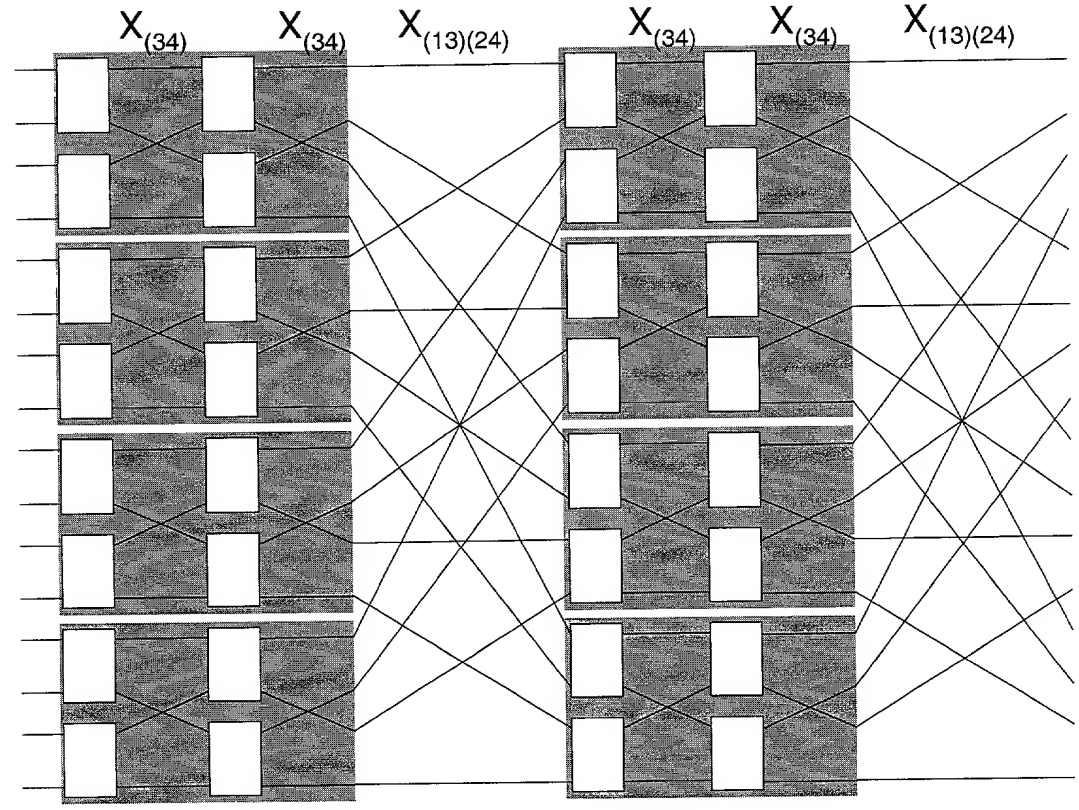
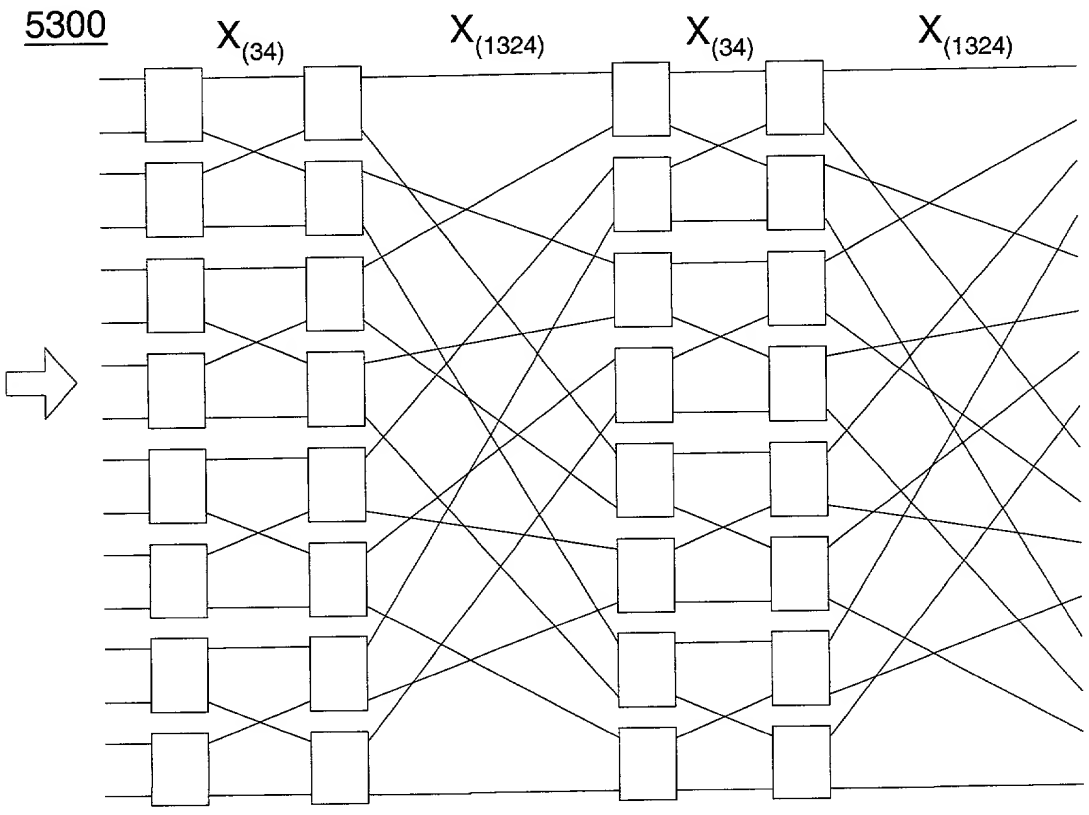



FIG. 52

FIG. 53



5400

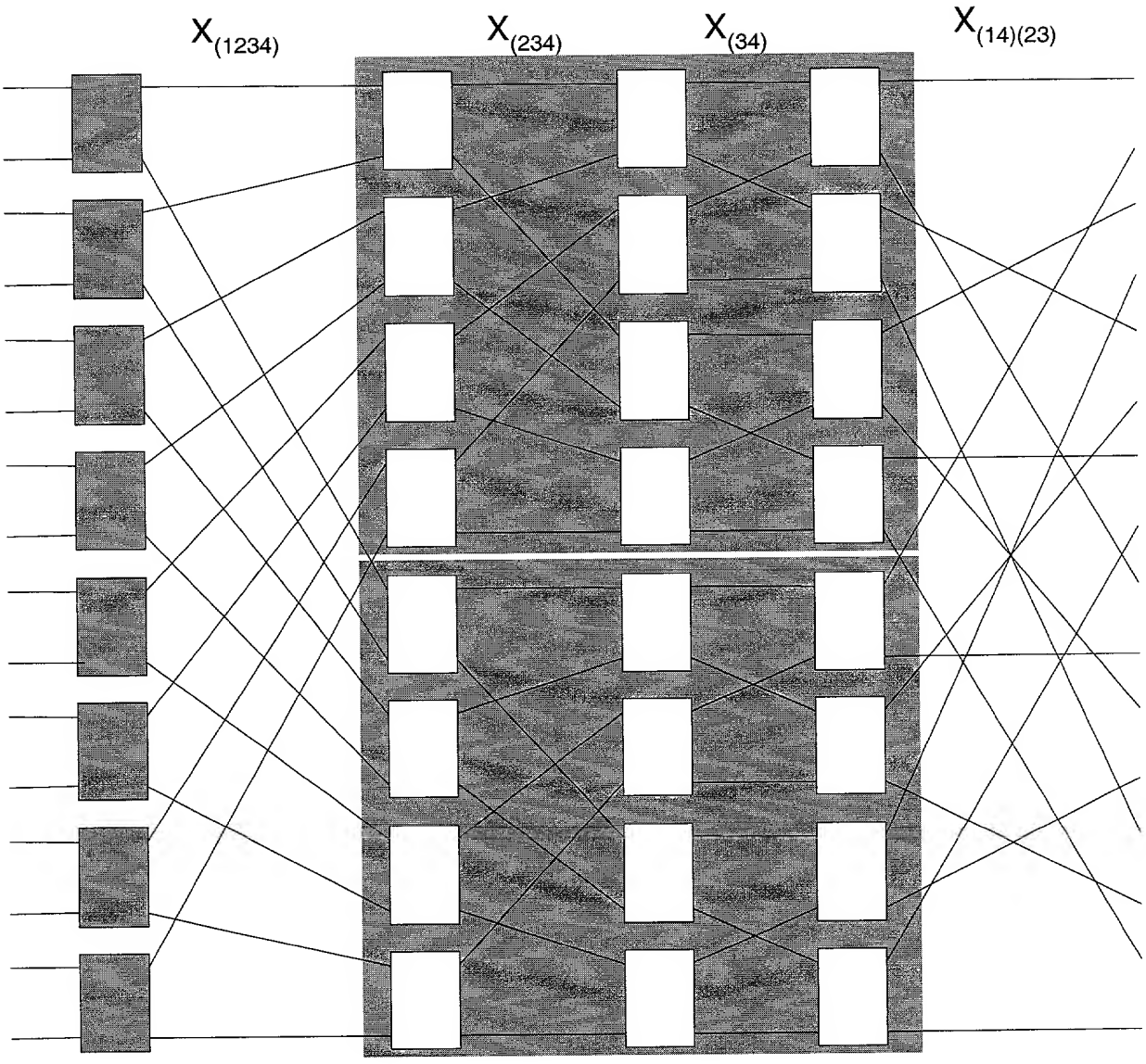



FIG. 54

FIG. 55

POSITA ASSIGNED

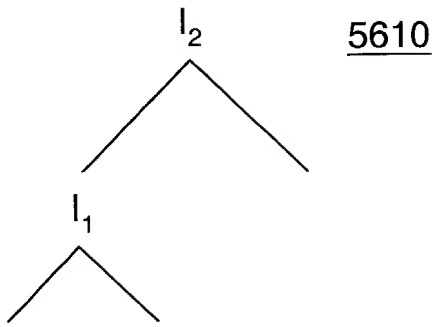



FIG. 56A

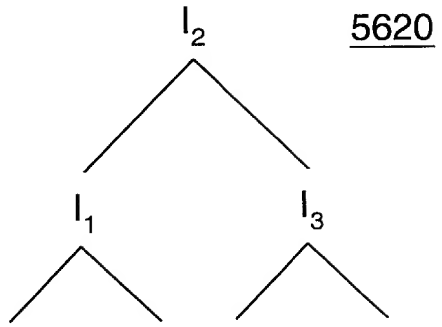



FIG. 56B

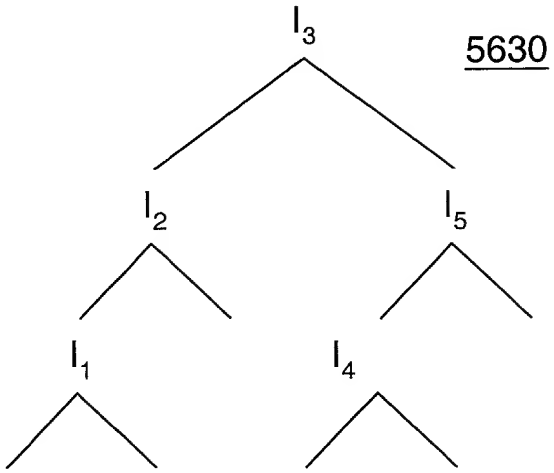



FIG. 56C

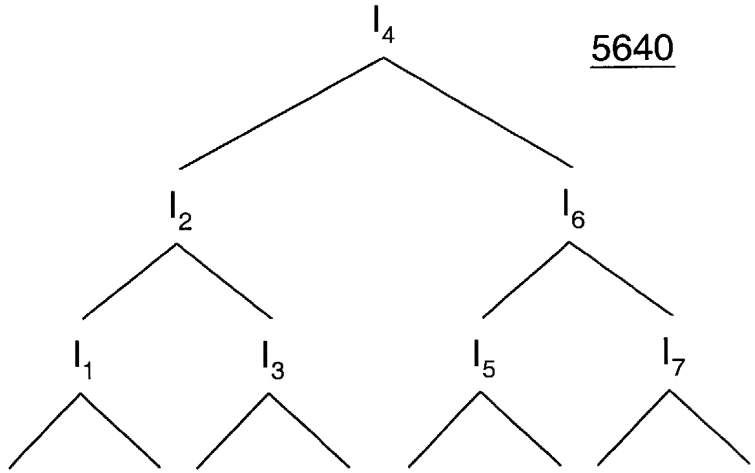
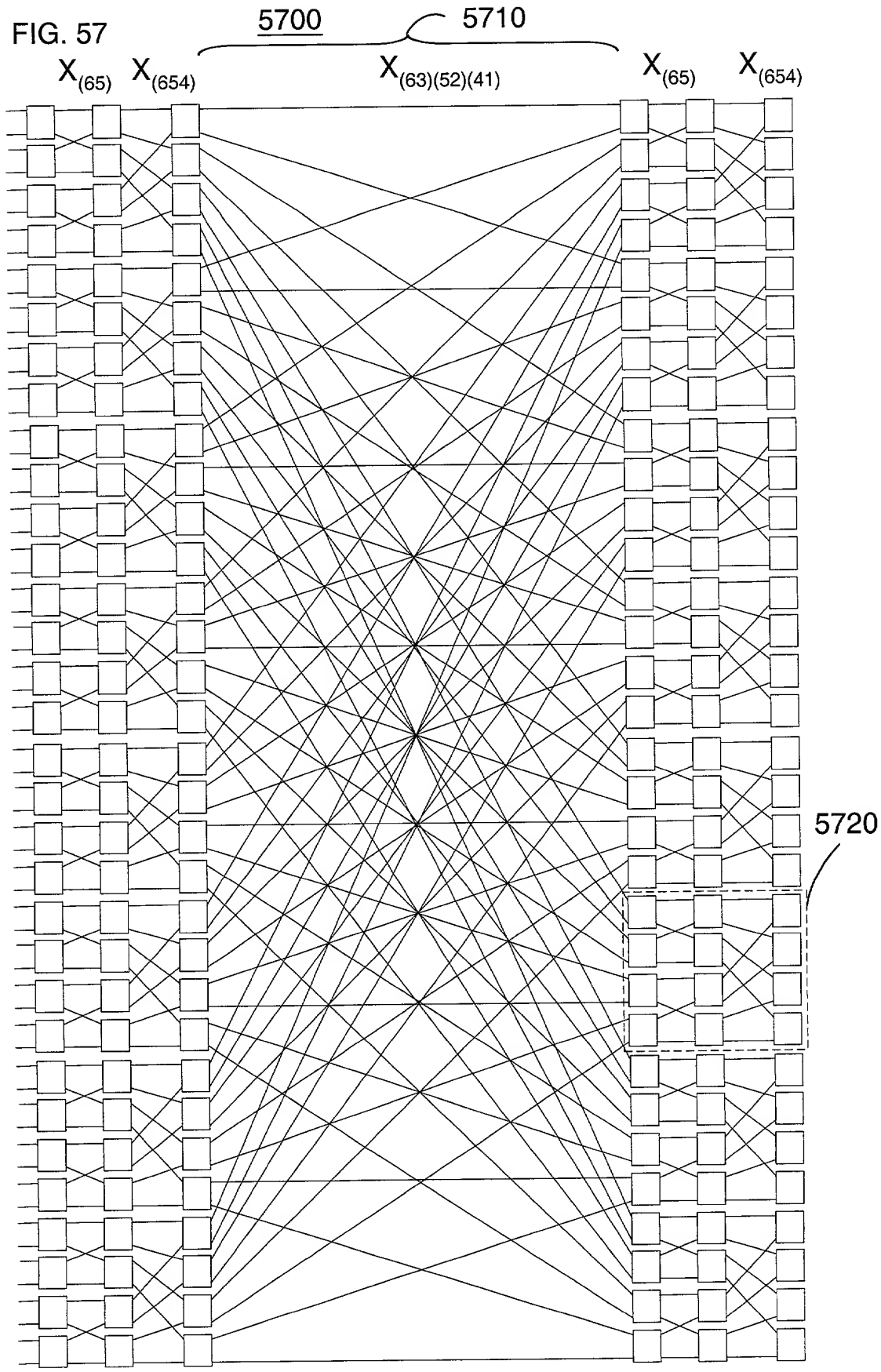



FIG. 56D

FIG. 57



PCT/SE2004/001813

FIG. 58

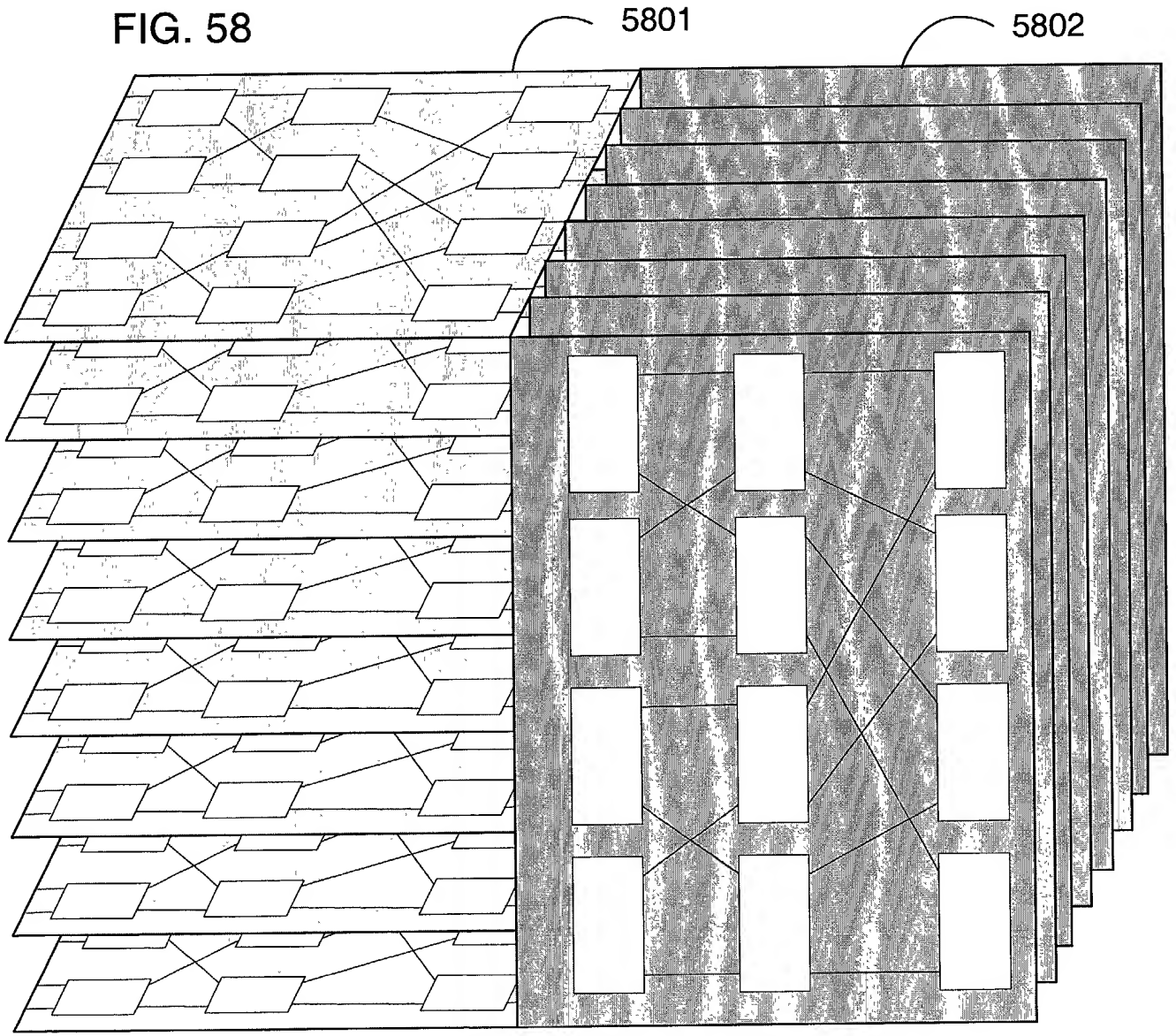
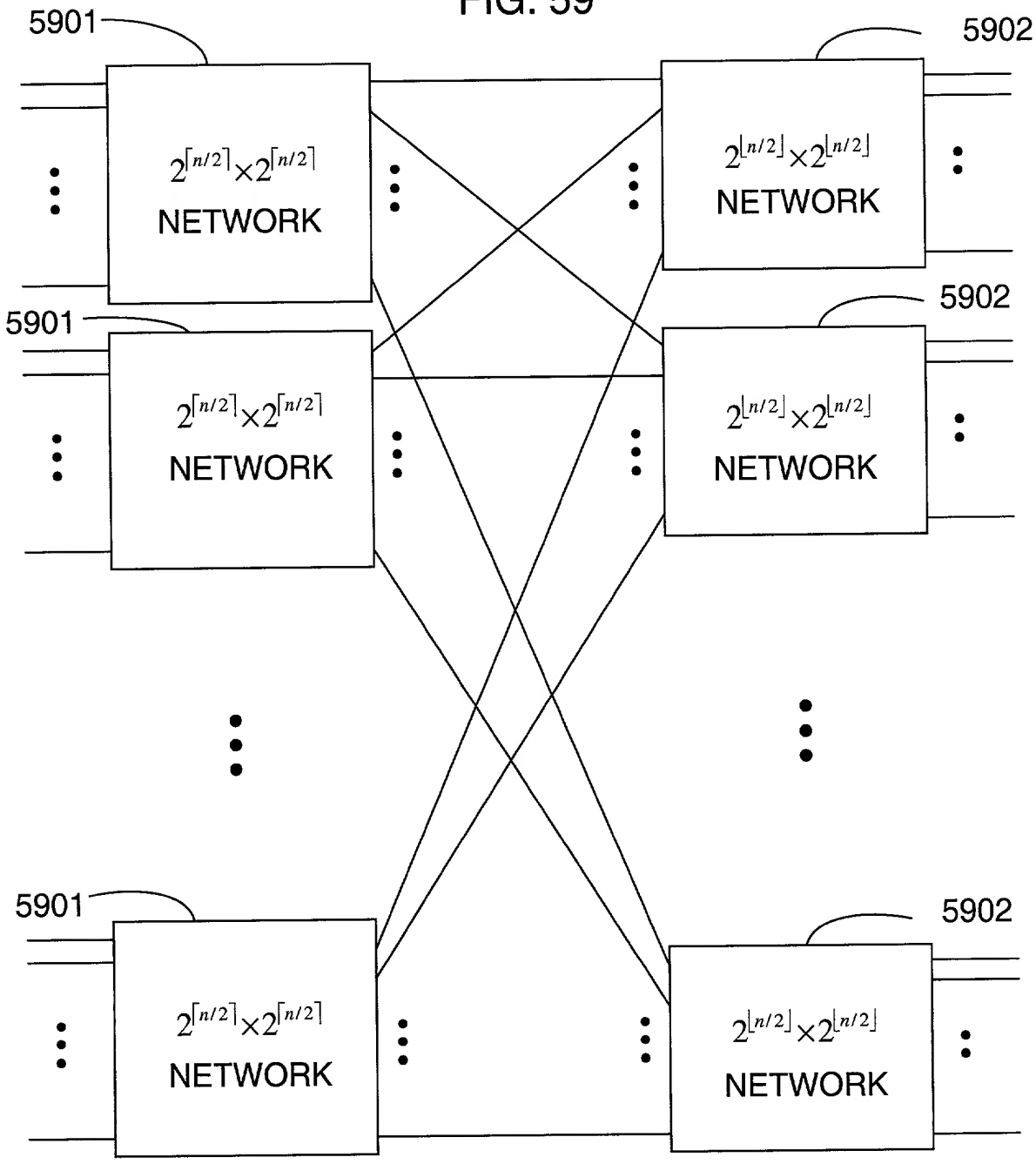


FIG. 59


5901
5902
$2^{\lceil n/2 \rceil} \times 2^{\lceil n/2 \rceil}$
NETWORK
$2^{\lfloor n/2 \rfloor} \times 2^{\lfloor n/2 \rfloor}$
NETWORK

Electronic Patent Application

6000

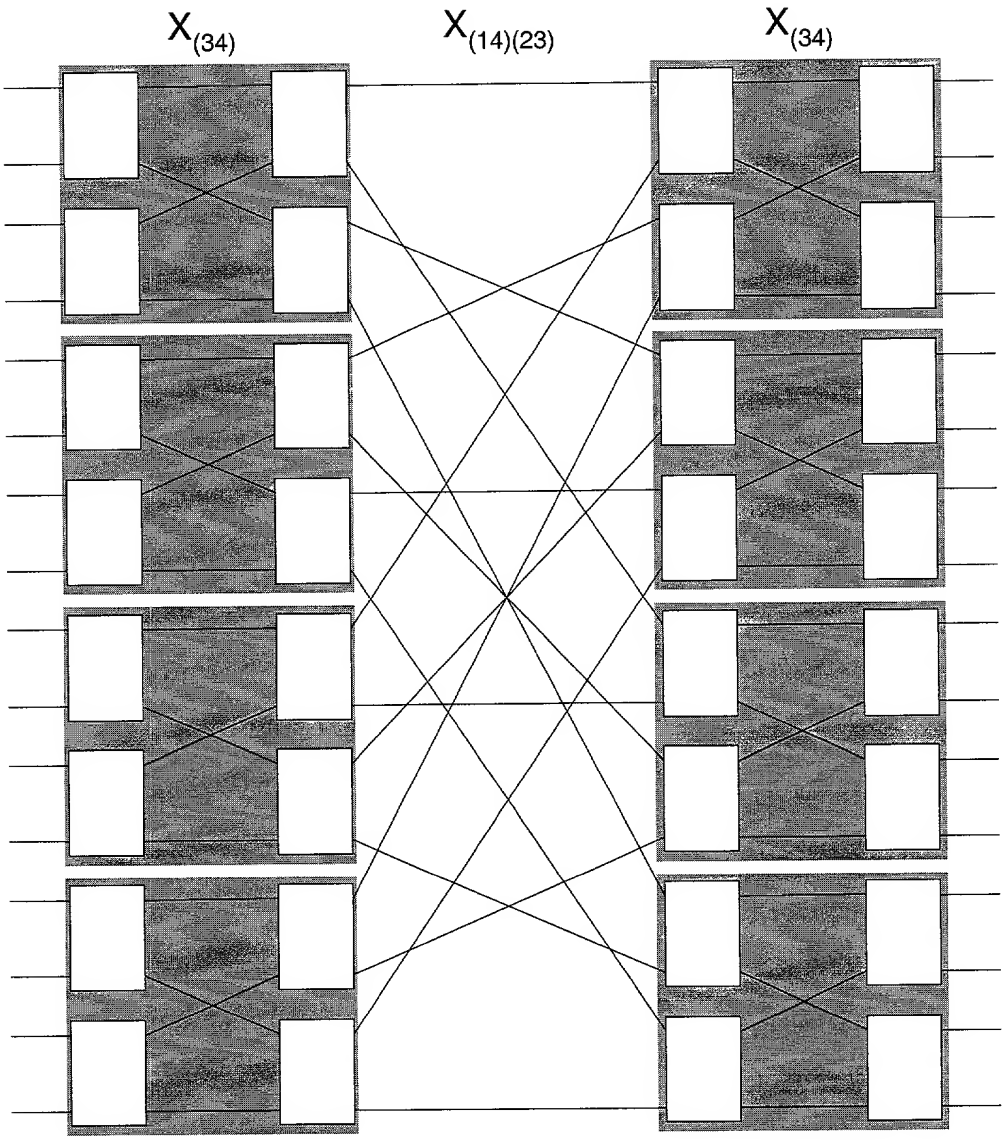
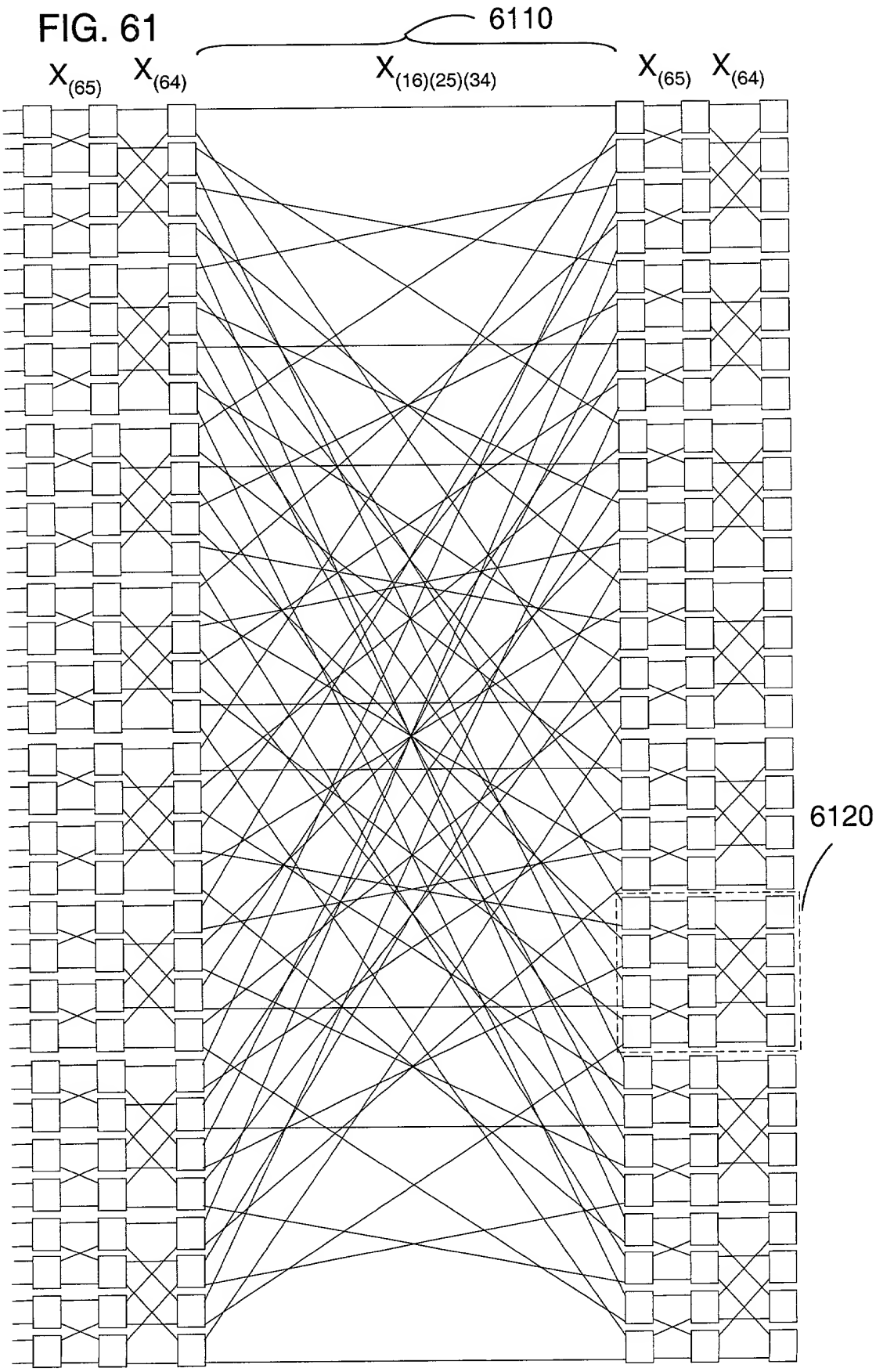



FIG. 60

FIG. 61



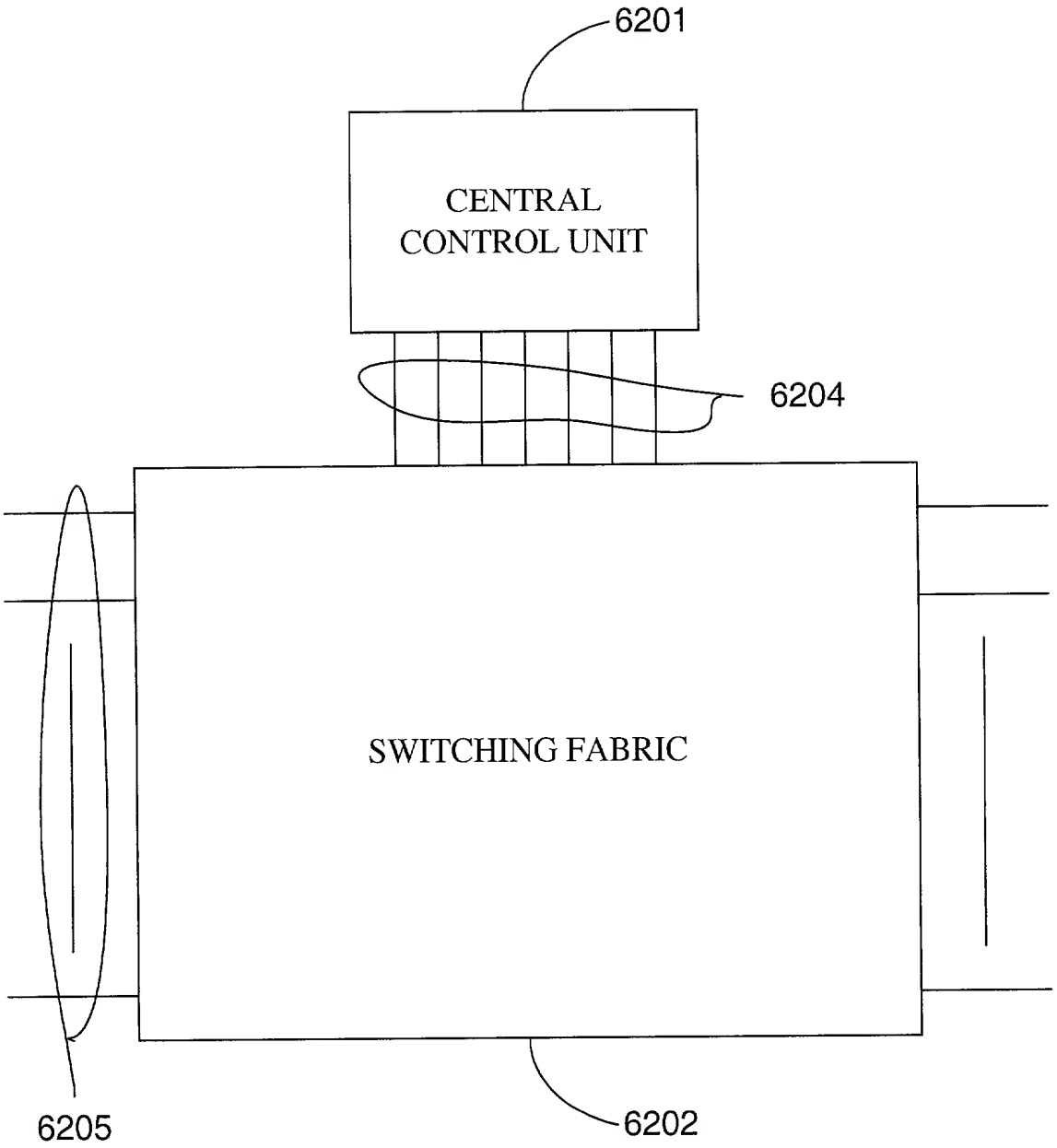



FIG. 62A

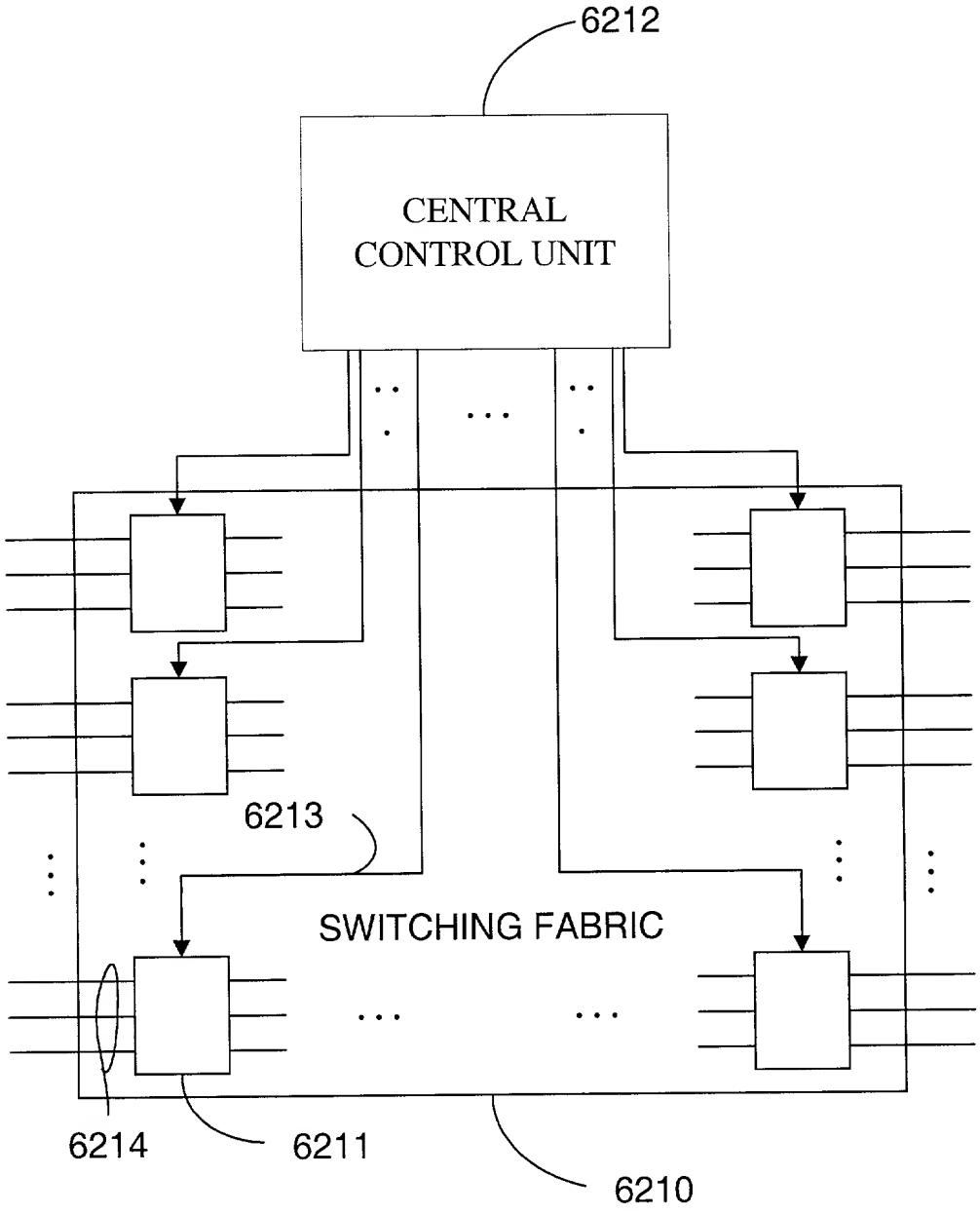

6212
CENTRAL
CONTROL UNIT
6213
SWITCHING FABRIC
6214
6211
6210

FIG. 62B

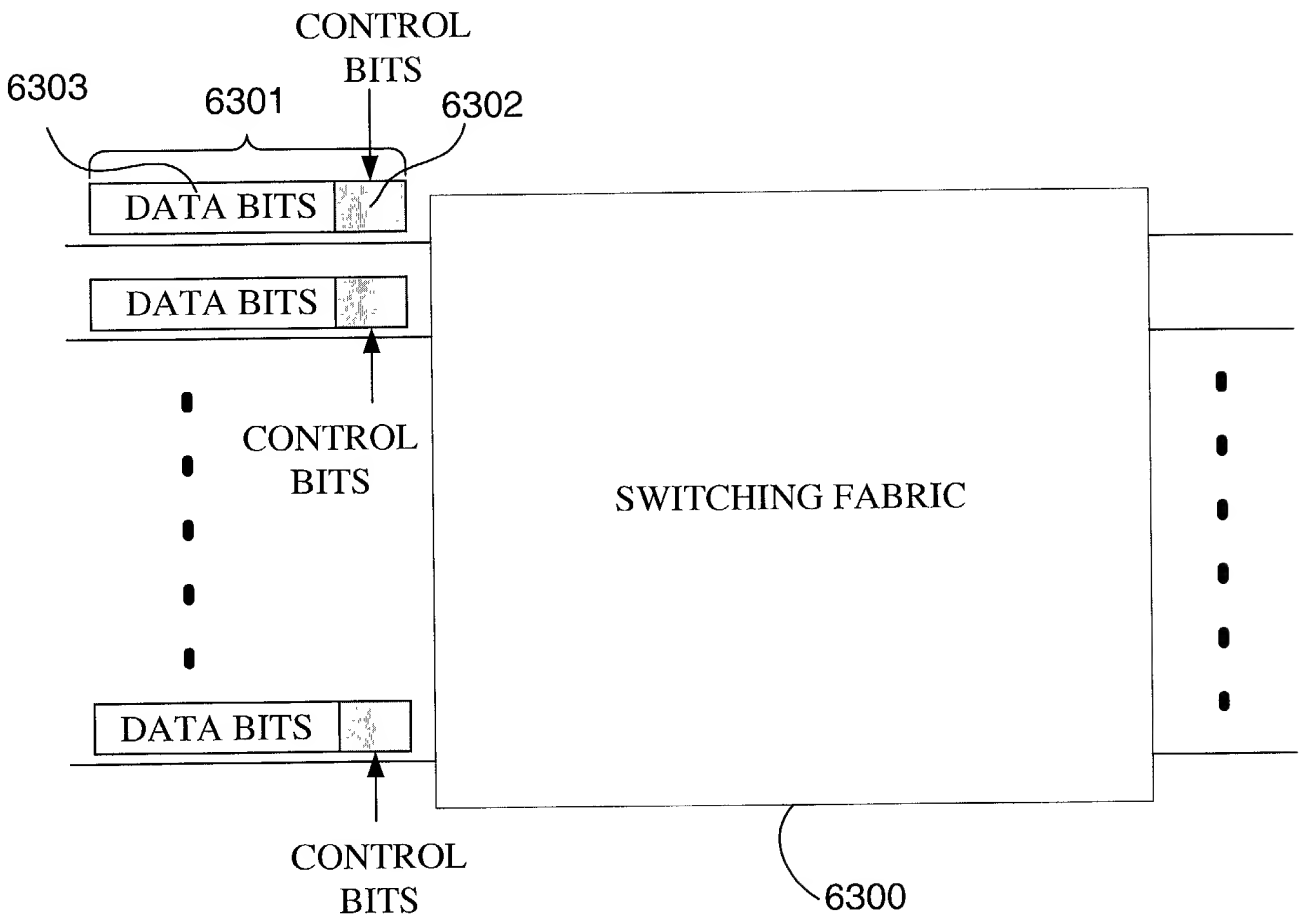

CONTROL
BITS
6303
6301
6302
DATA BITS
DATA BITS
CONTROL
BITS
SWITCHING FABRIC
DATA BITS
CONTROL
BITS
6300

FIG. 63A

Patent Application

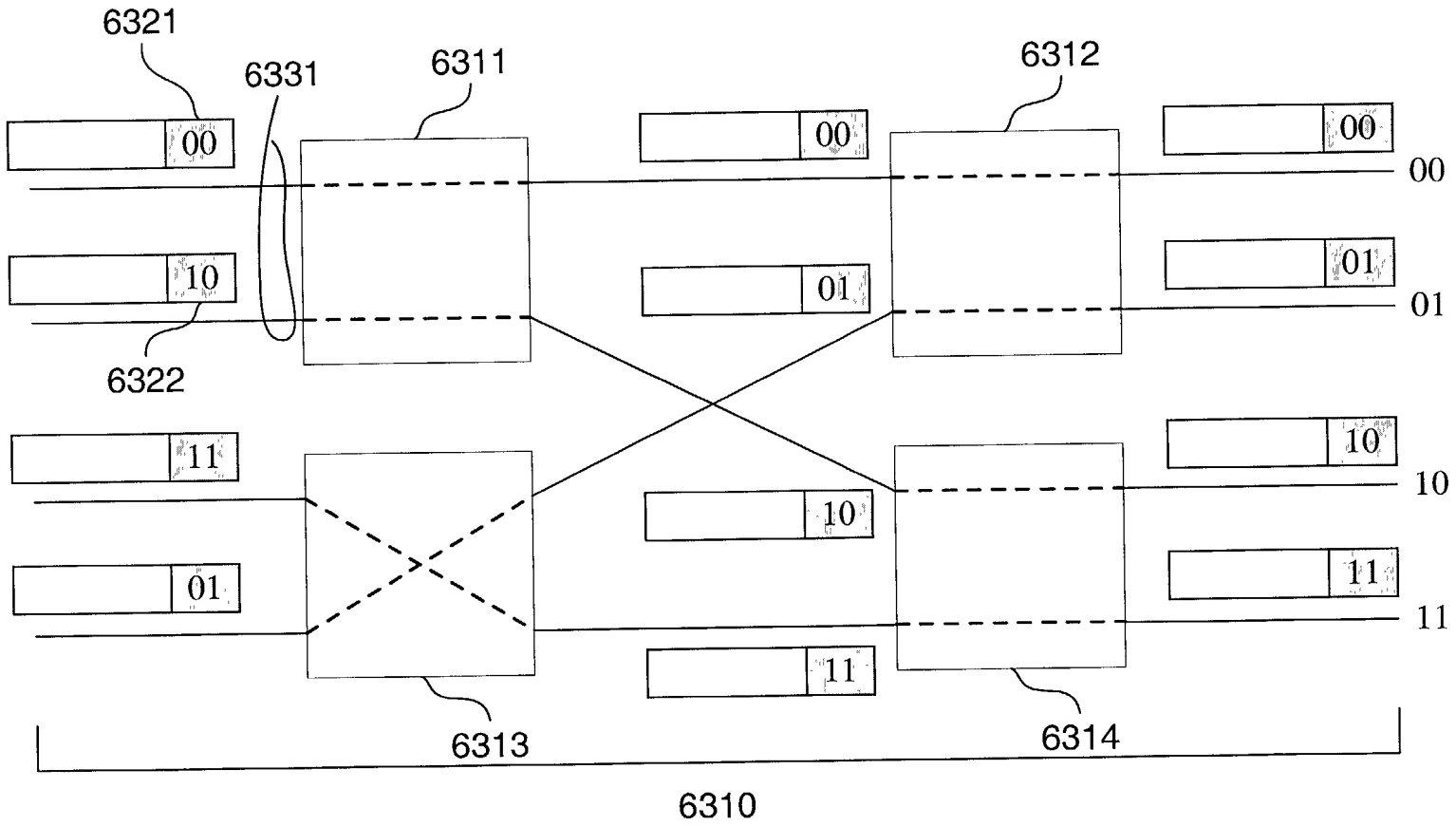



FIG. 63B

TOSHIBA 2000

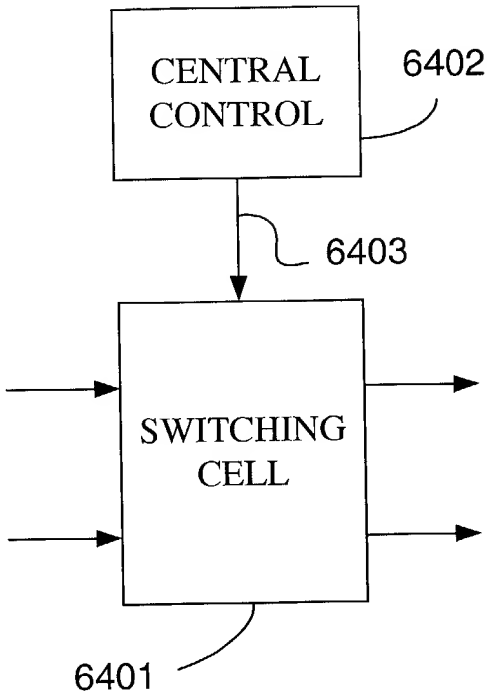



FIG. 64A

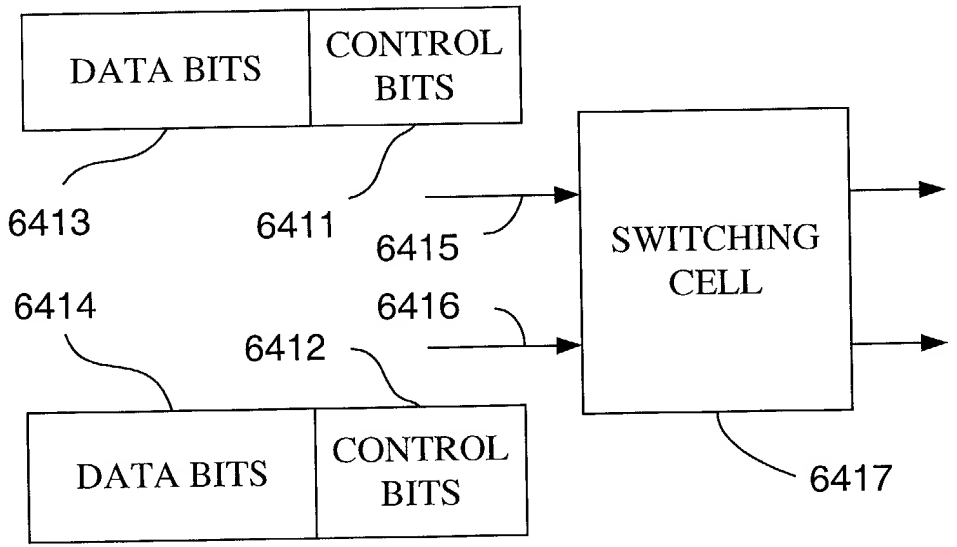



FIG. 64B

Patent Application

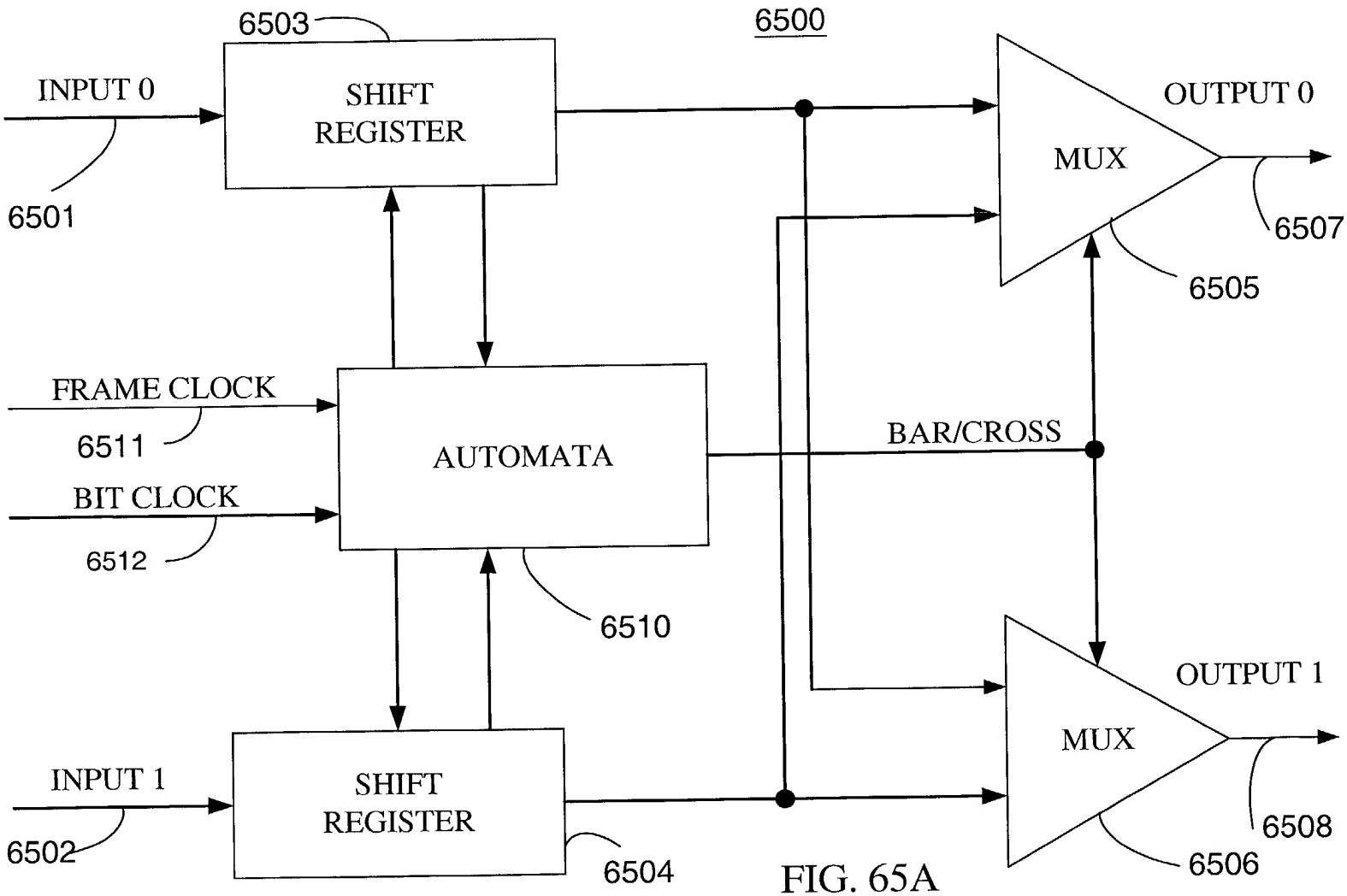



FIG. 65A

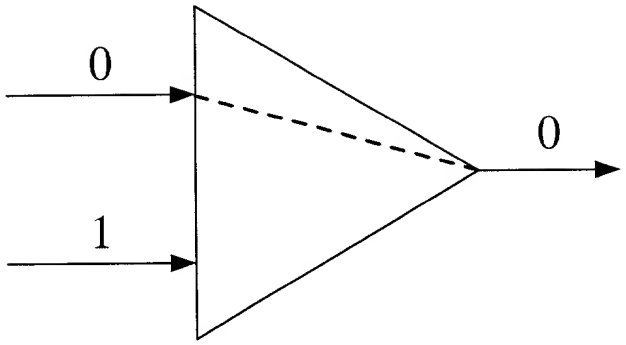



FIG. 65B

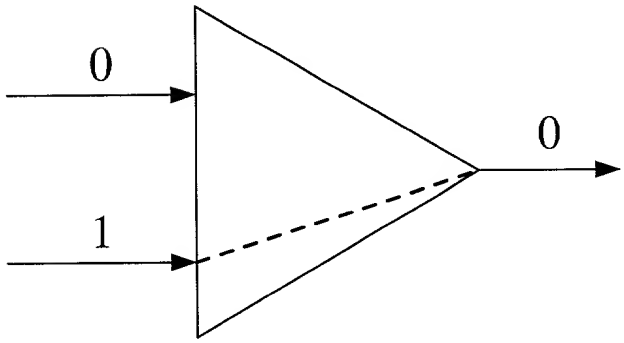



FIG. 65C

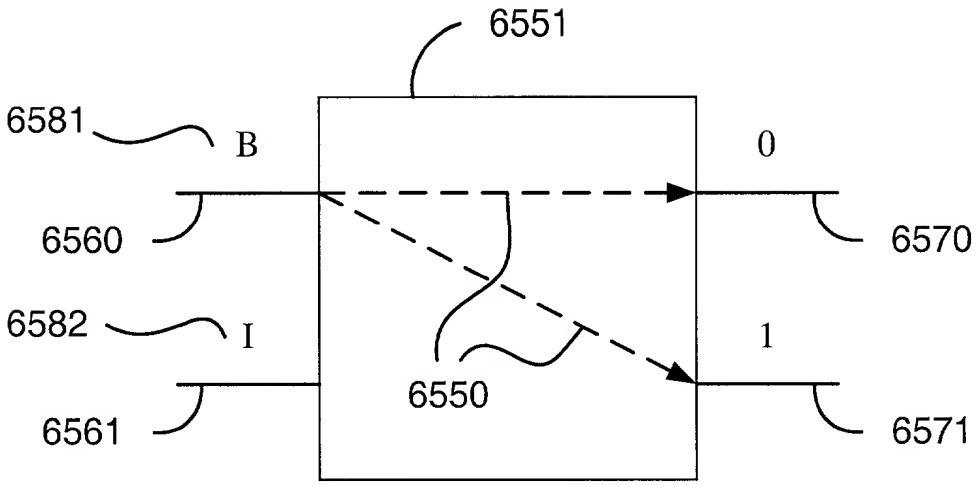



FIG. 65D

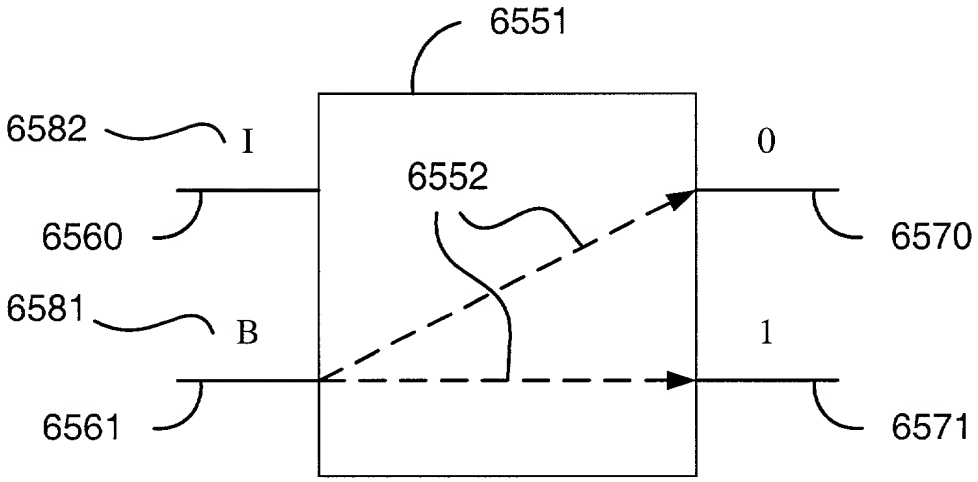



FIG. 65E

POSITA - 2851-0850.03

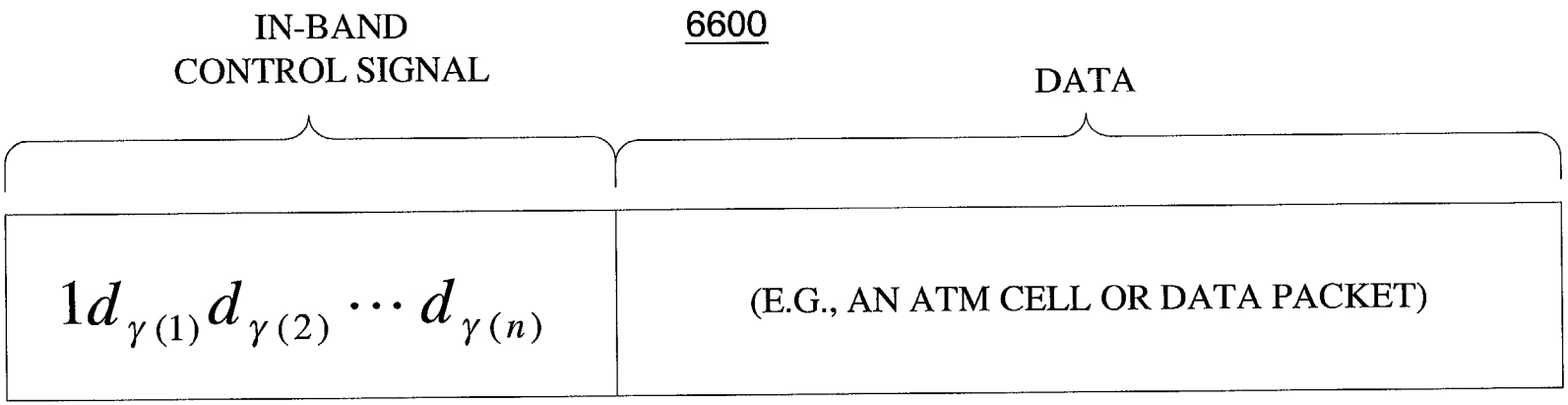



FIG. 66A

Postal Postcard

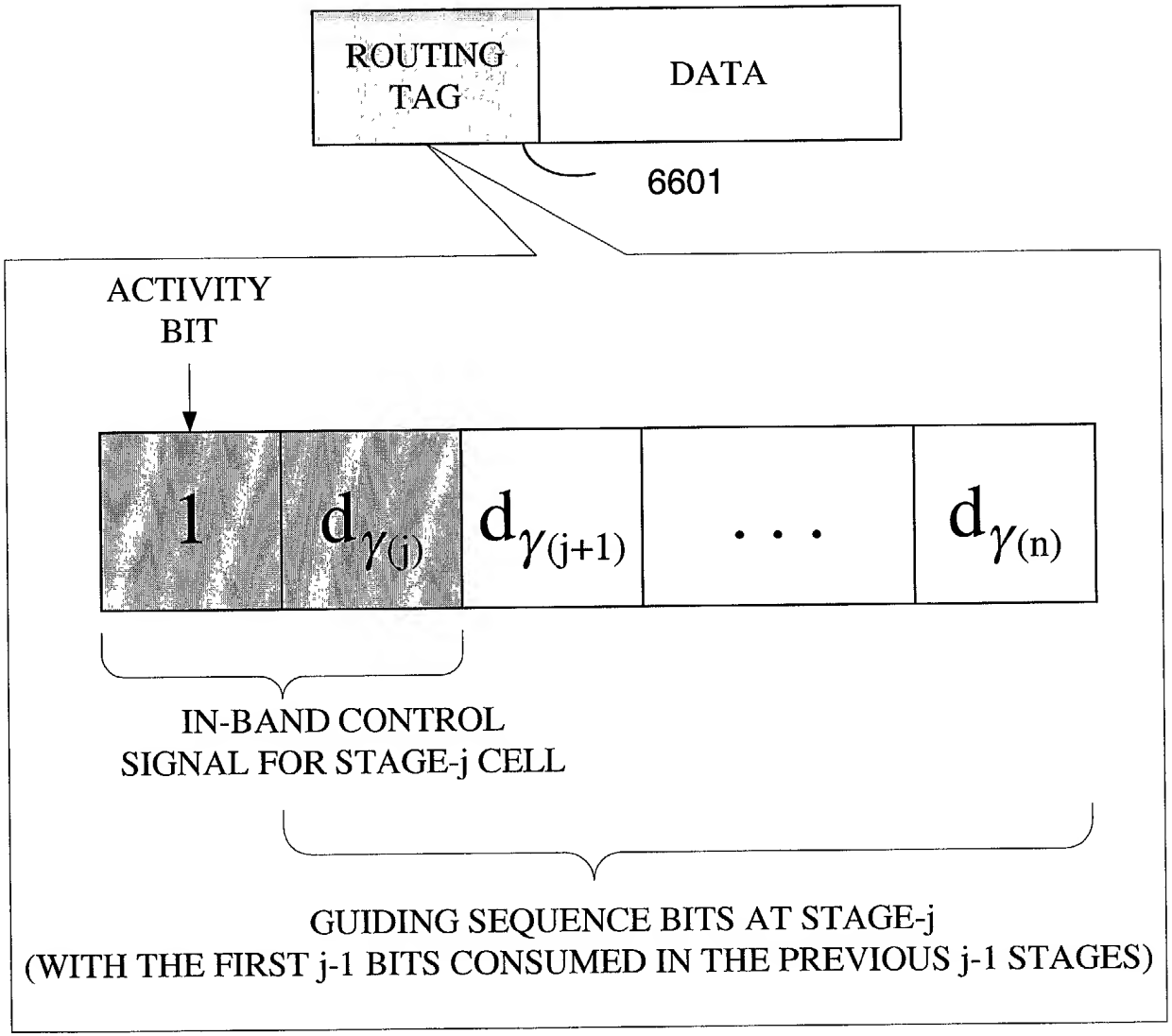



FIG. 66B

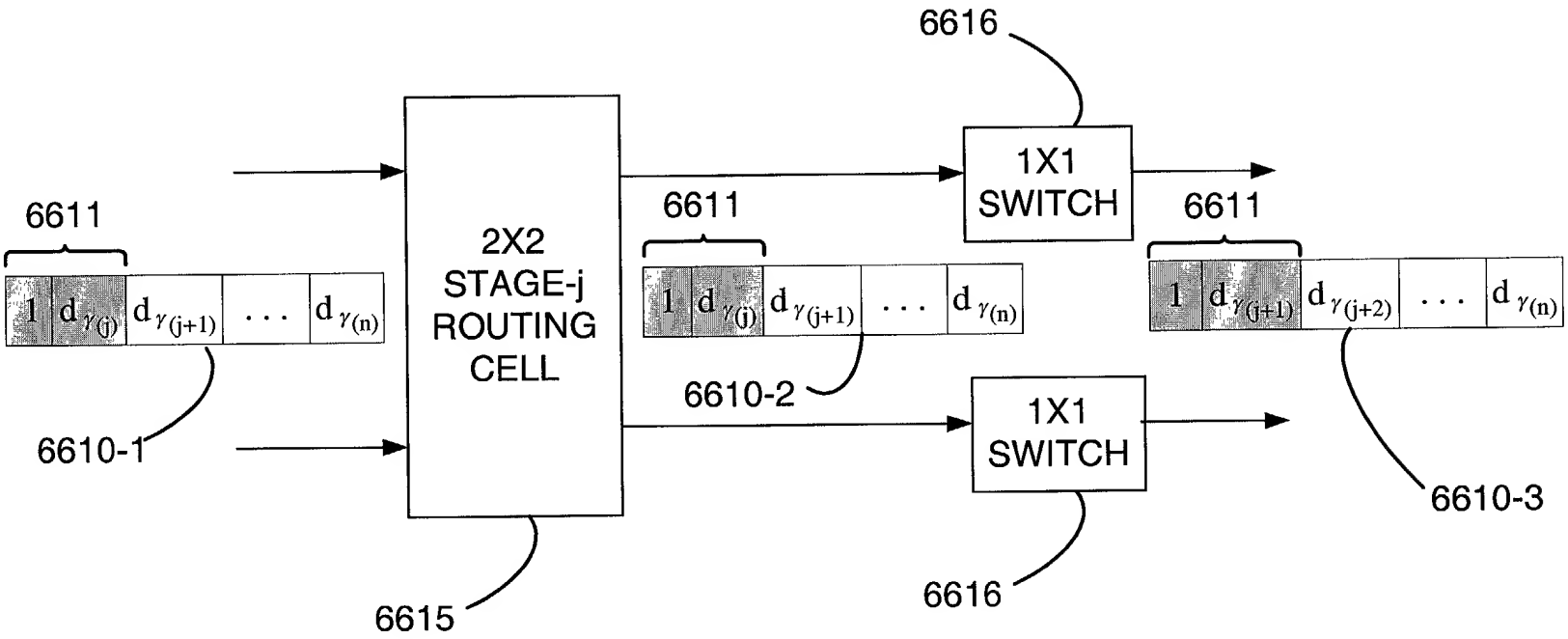

6611
1
d γ(j)
d γ(j+1)
. . .
d γ(n)
6610-1
2X2
STAGE-j
ROUTING
CELL
6615
6616
1X1
SWITCH
6611
1
d γ(j)
d γ(j+1)
. . .
d γ(n)
6610-2
1X1
SWITCH
6616
6611
1
d γ(j+1)
d γ(j+2)
. . .
d γ(n)
6610-3

FIG. 66C

FIG. 66D

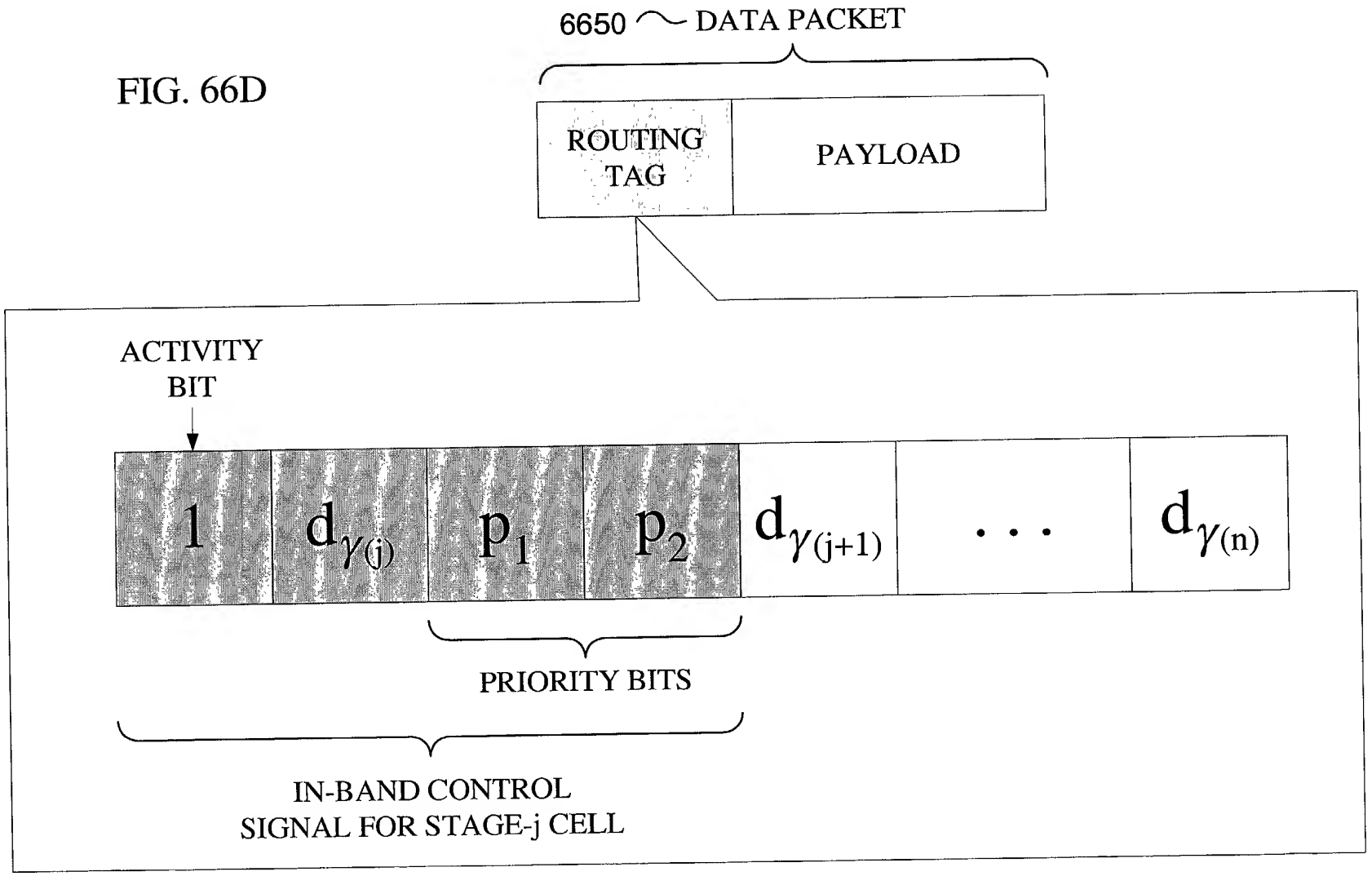

6650
DATA PACKET
ROUTING TAG
PAYLOAD
ACTIVITY BIT
1
$d_{\gamma(j)}$
$p_1$
$p_2$
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
PRIORITY BITS
IN-BAND CONTROL SIGNAL FOR STAGE-j CELL

FIG. 67A

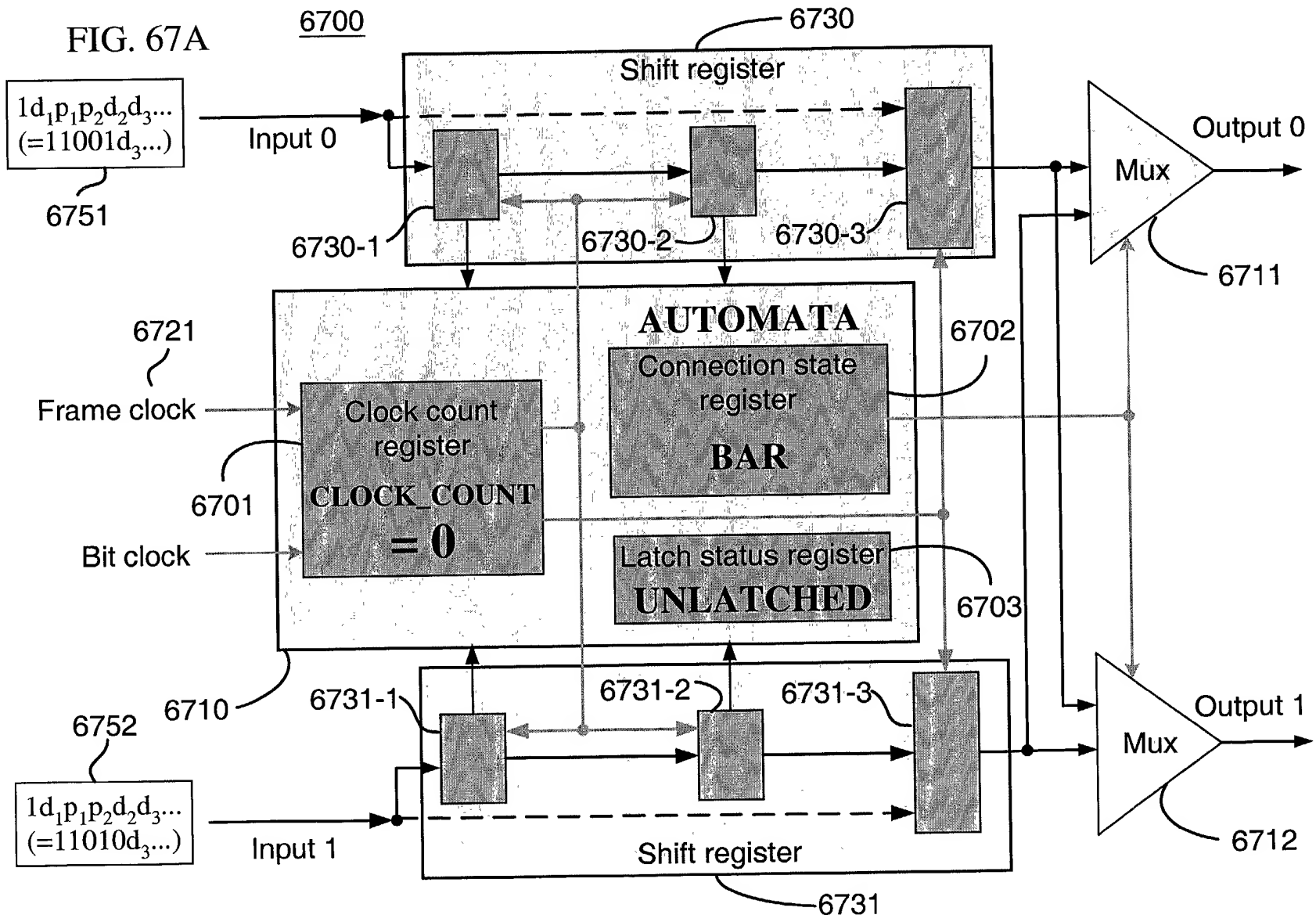

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
6730-1
6730-2
6730-3
Output 0
Mux
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 0
Connection state register
BAR
6702
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731
6712

FIG. 67B

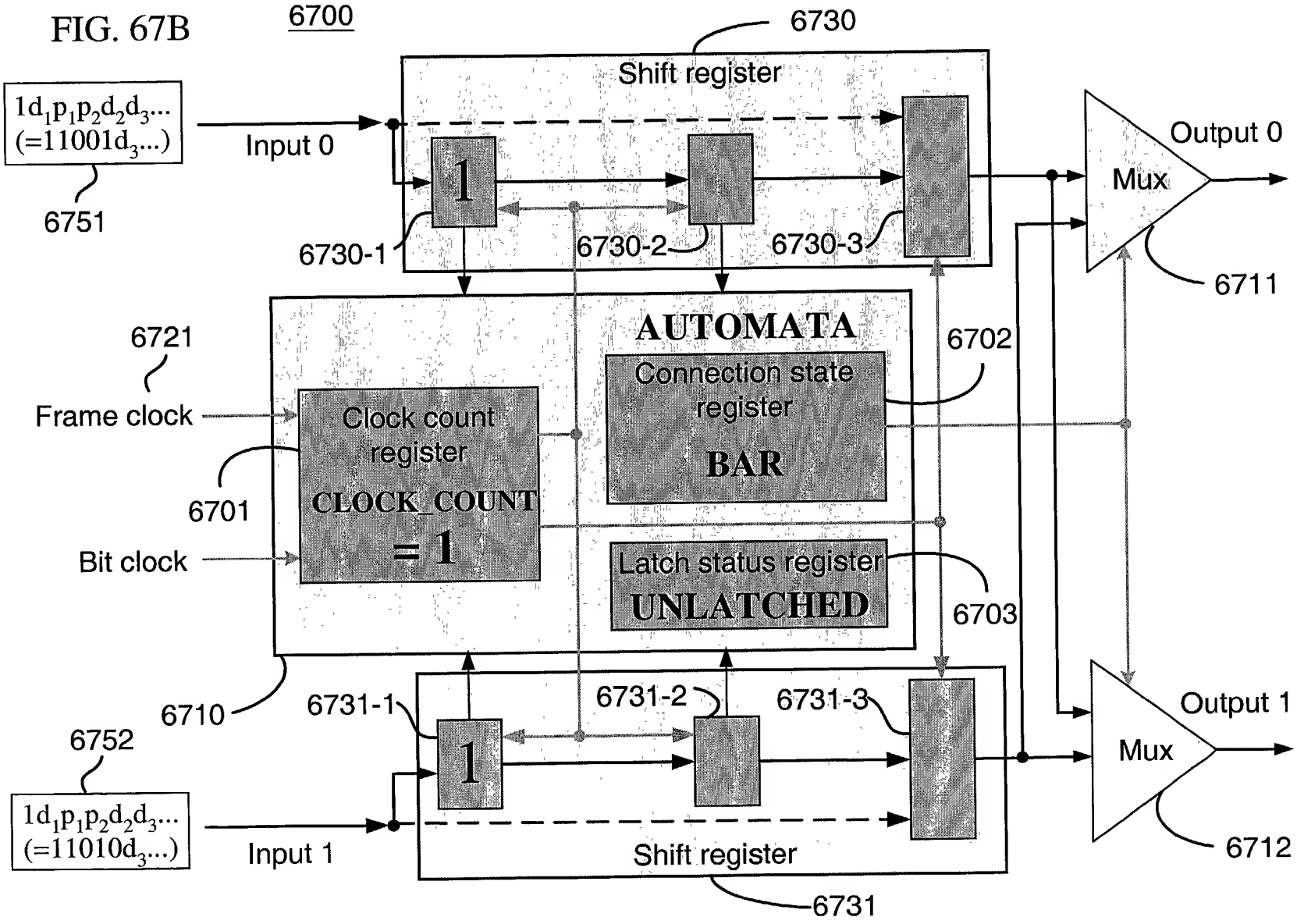

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
6702
Connection state register
BAR
Clock count register
CLOCK_COUNT
= 1
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731
6712

FIG. 67C

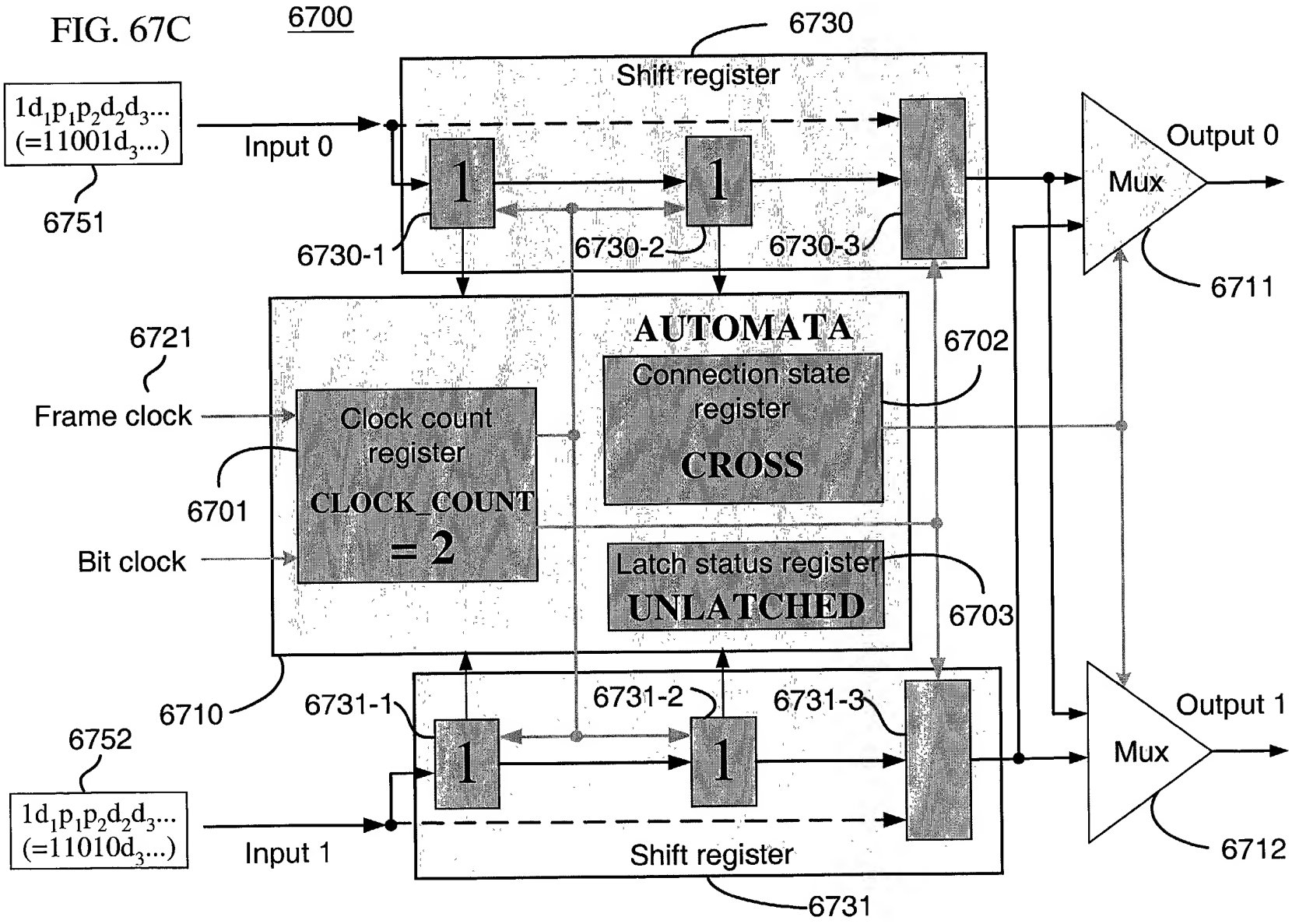

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
1
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 2
6701
Bit clock
Connection state register
CROSS
6702
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731
6712

FIG. 67D

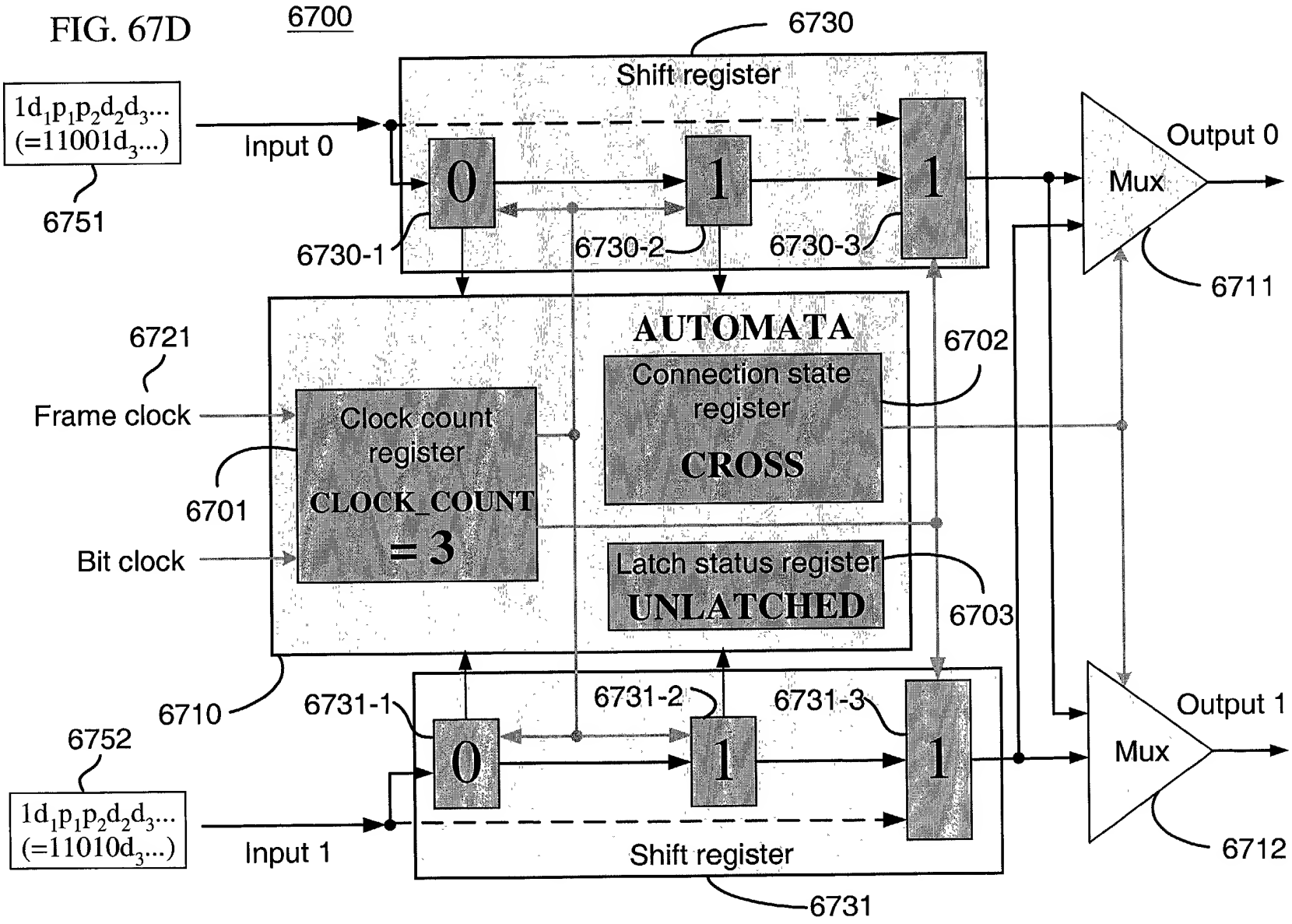

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
0
1
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 3
6701
Bit clock
Connection state register
CROSS
6702
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
0
1
1
Output 1
Mux
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731
6712

FIG. 67E

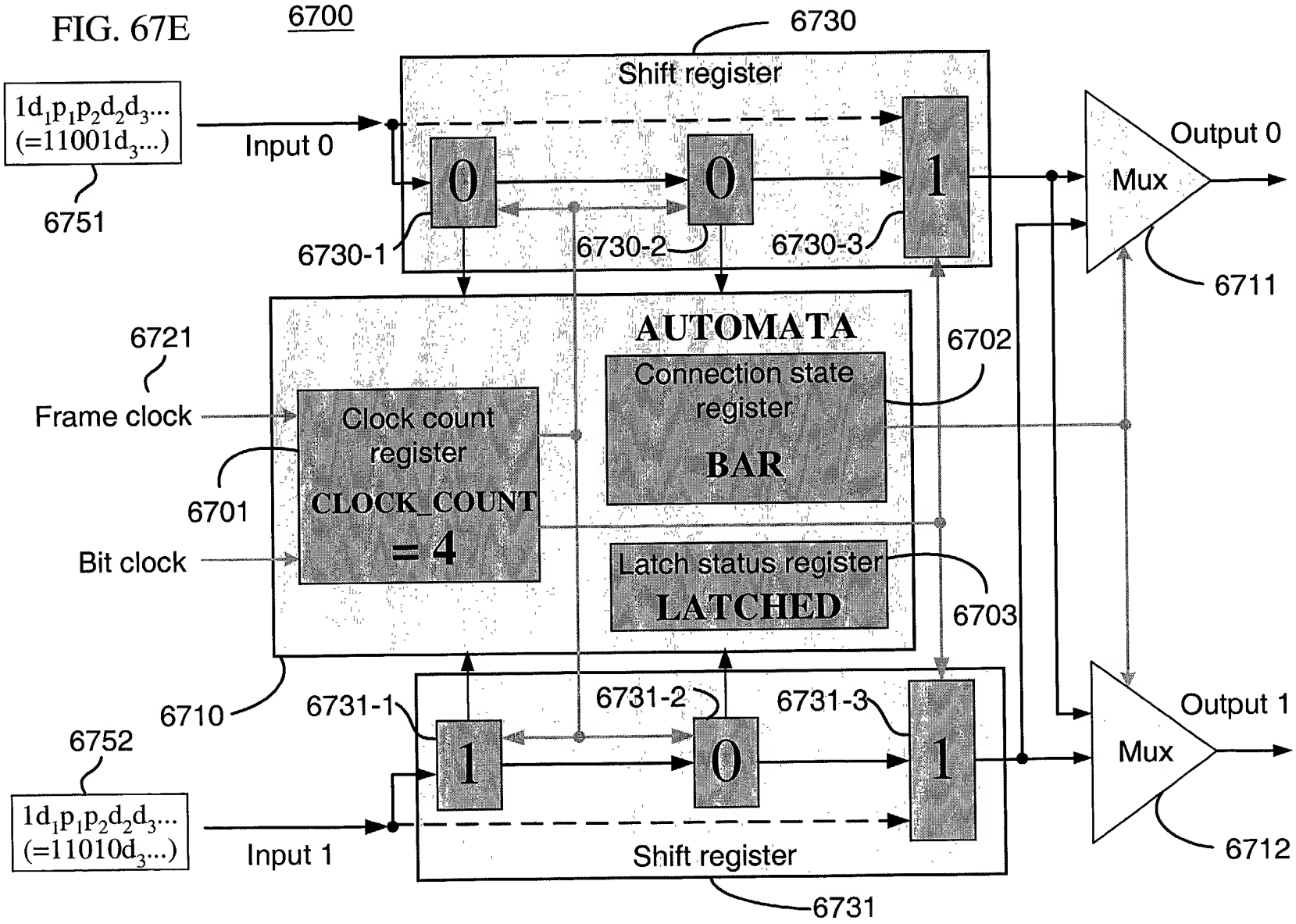
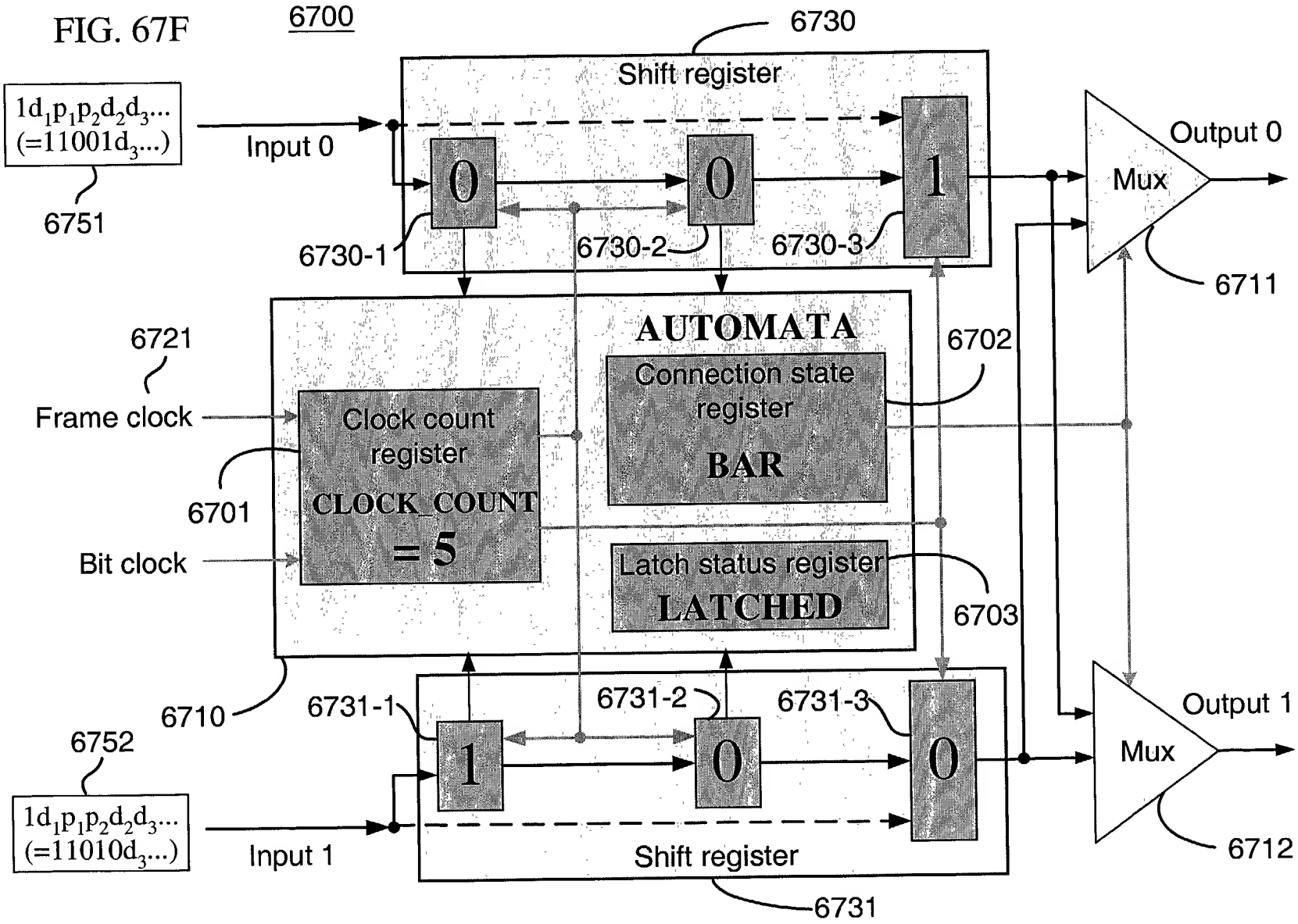

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
0
0
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 4
6701
Bit clock
Connection state register
BAR
6702
Latch status register
LATCHED
6703
6710
6731-1
6731-2
6731-3
1
0
1
Output 1
Mux
6712
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731

FIG. 67F


6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
Input 0
6751
0
0
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 5
6701
Bit clock
Connection state register
BAR
6702
Latch status register
LATCHED
6703
6710
6731-1
6731-2
6731-3
1
0
0
Output 1
Mux
6712
6752
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6731

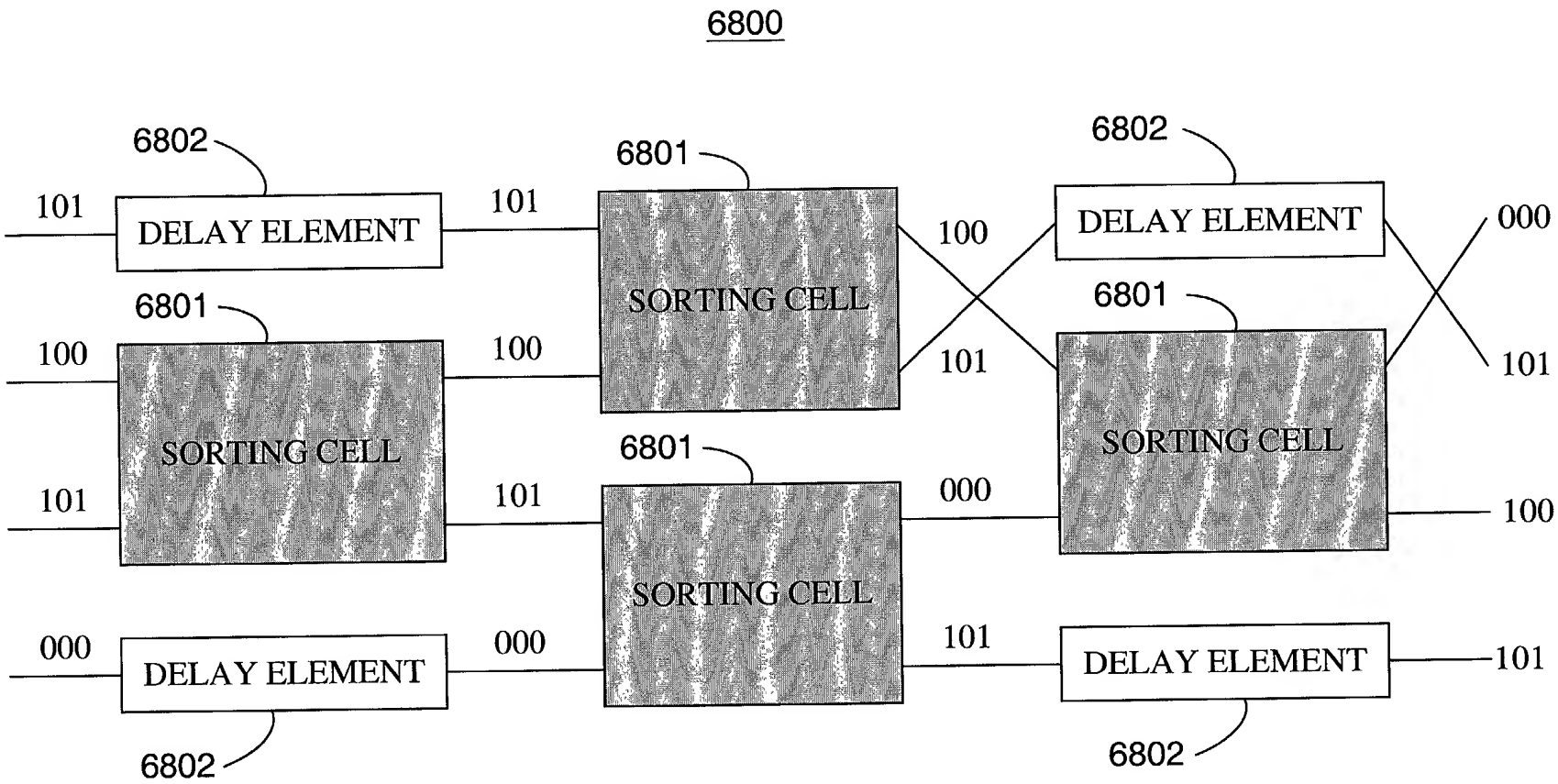
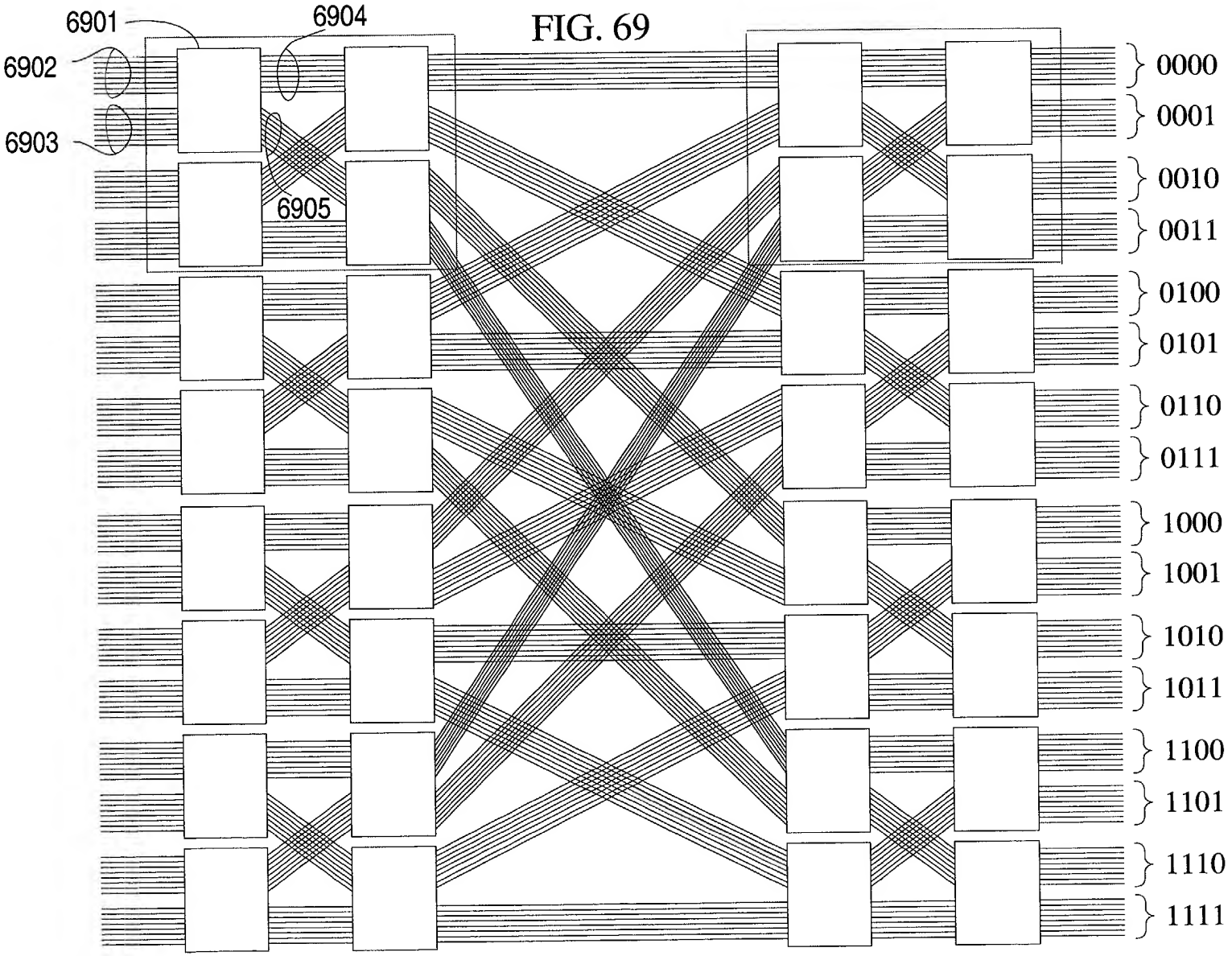

6800
6802
6801
6802
101
DELAY ELEMENT
101
100
DELAY ELEMENT
000
6801
6801
100
SORTING CELL
100
101
SORTING CELL
101
6801
101
SORTING CELL
101
000
100
SORTING CELL
000
DELAY ELEMENT
000
101
DELAY ELEMENT
101
6802
6802

FIG. 68

FIG. 69


6901
6904
6902
6903
6905
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

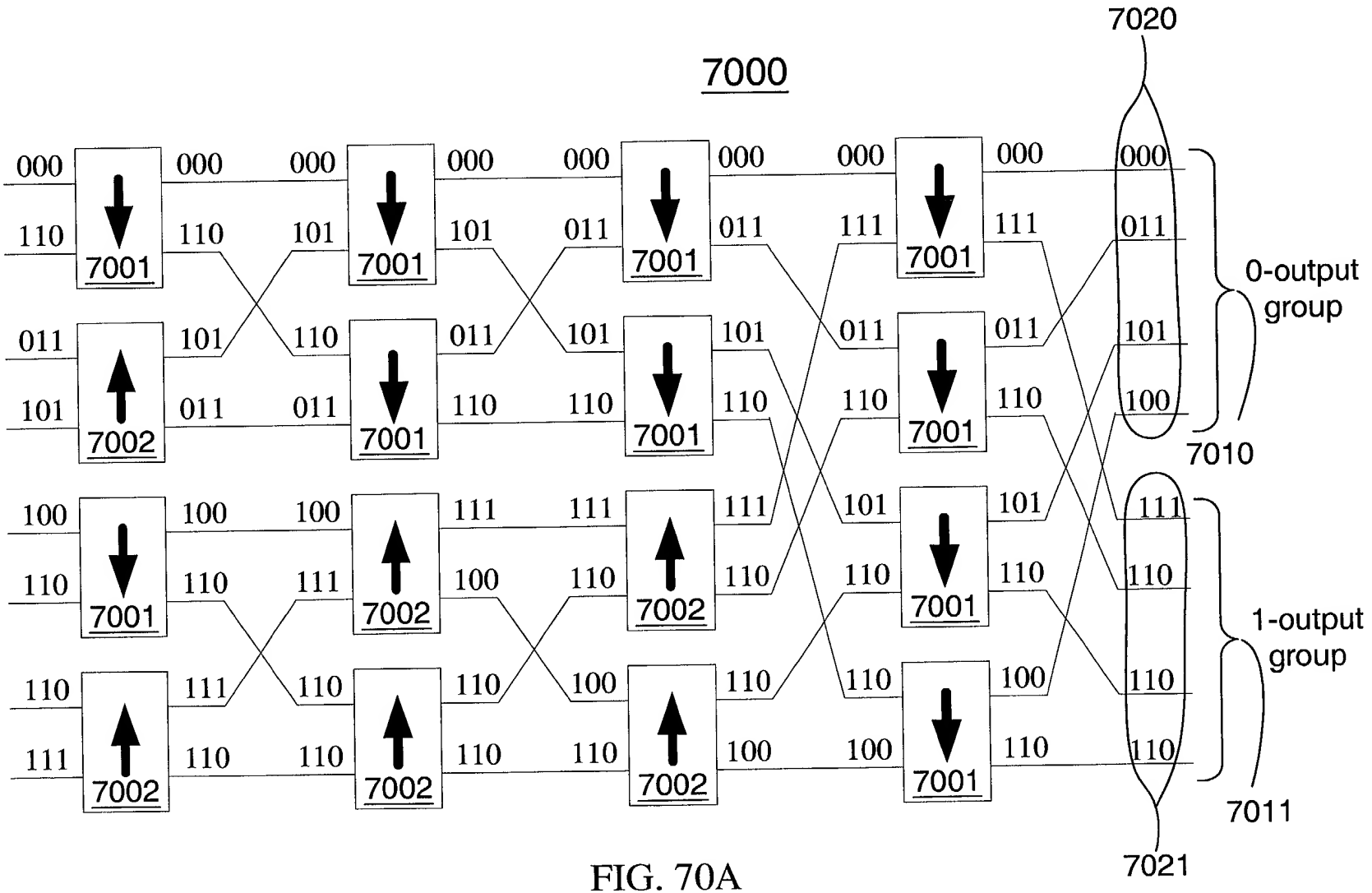

7000
7020
7001
7002
0-output group
1-output group
7010
7011
7021

FIG. 70A

Patent Application

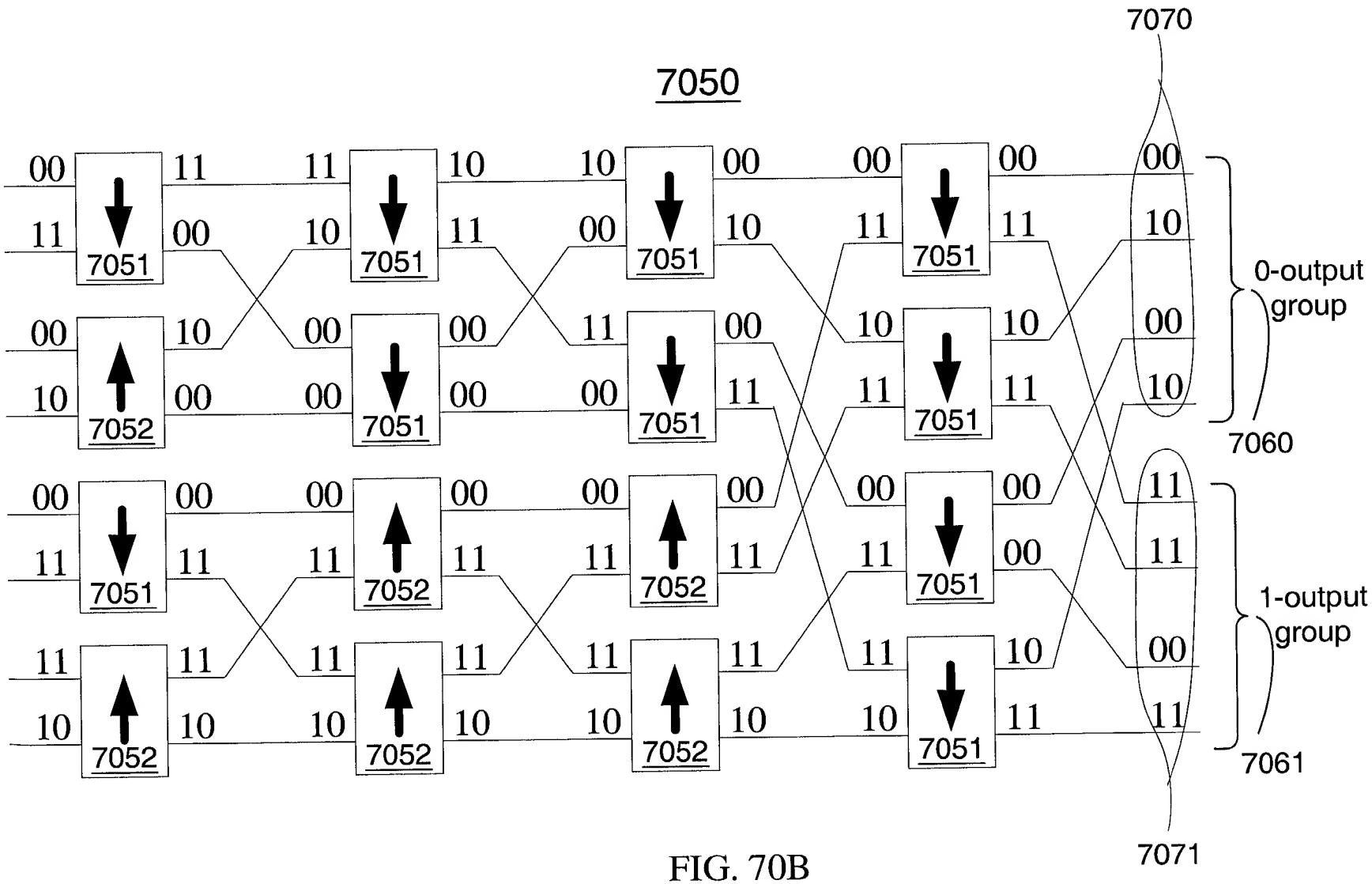



FIG. 70B

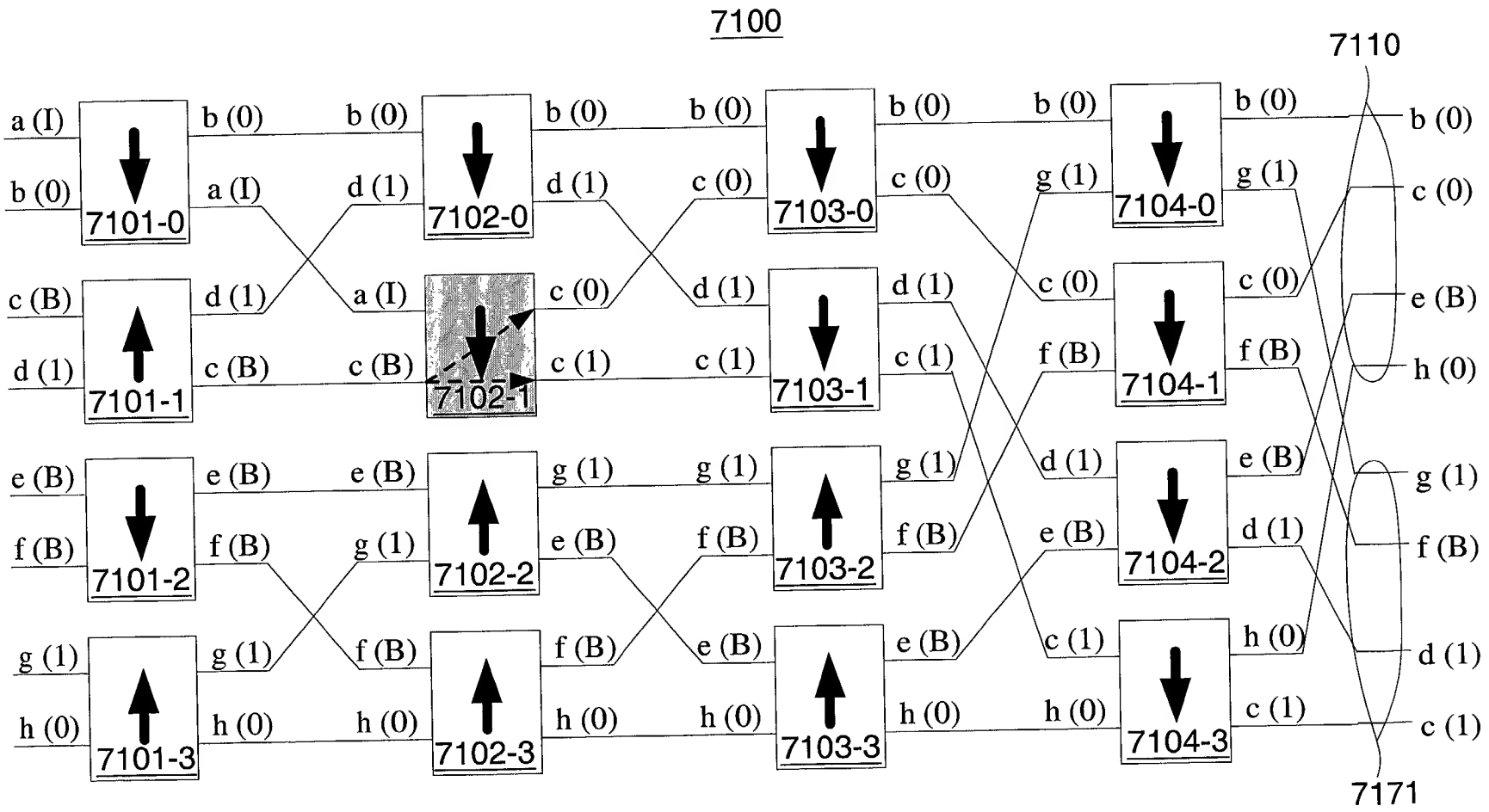

7100
7110
7171
7101-0
7101-1
7101-2
7101-3
7102-0
7102-1
7102-2
7102-3
7103-0
7103-1
7103-2
7103-3
7104-0
7104-1
7104-2
7104-3
a (I)
b (0)
c (B)
d (1)
e (B)
f (B)
g (1)
h (0)
c (1)

FIG. 71A

Postal Certified

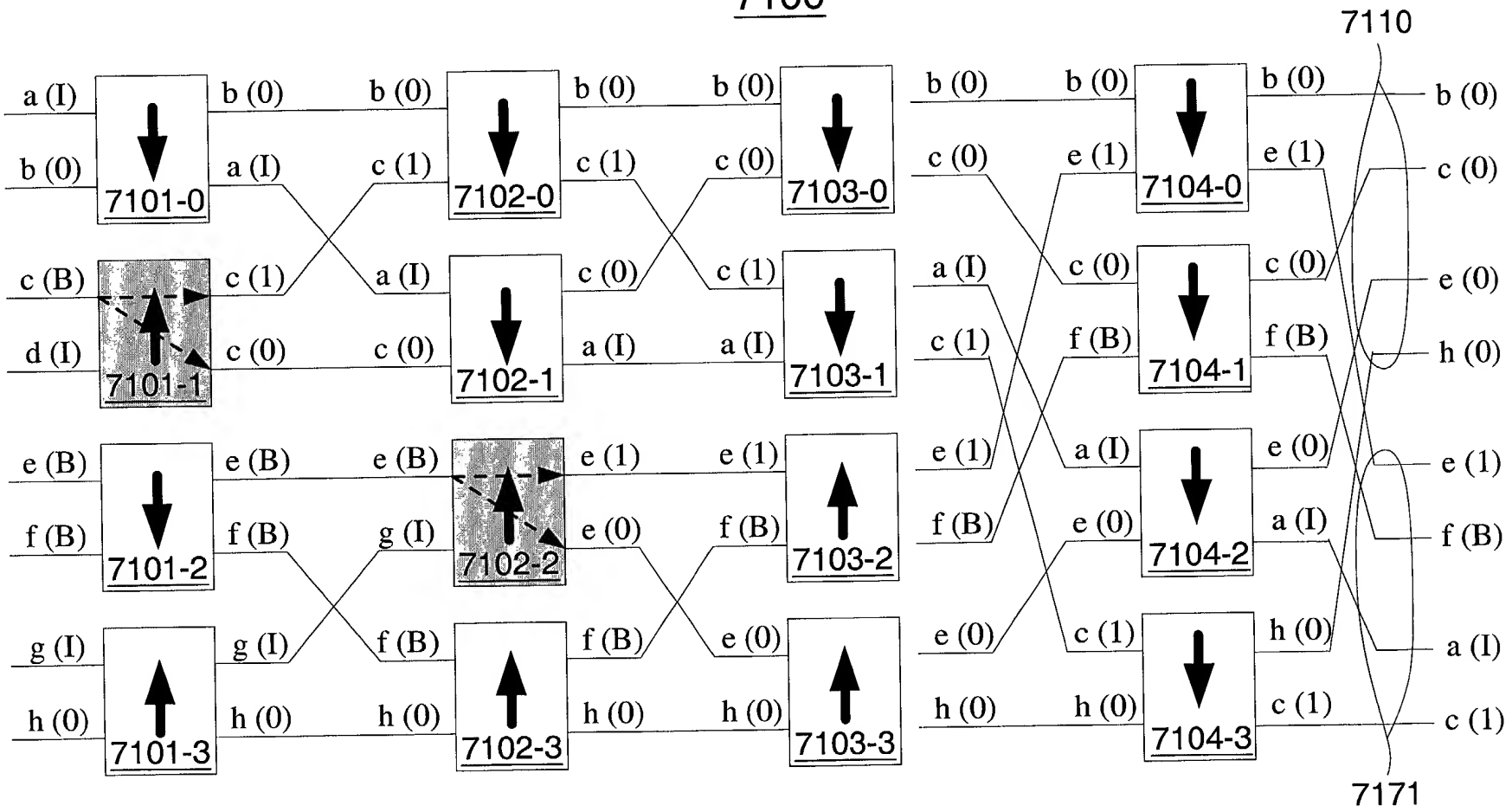



FIG. 71B

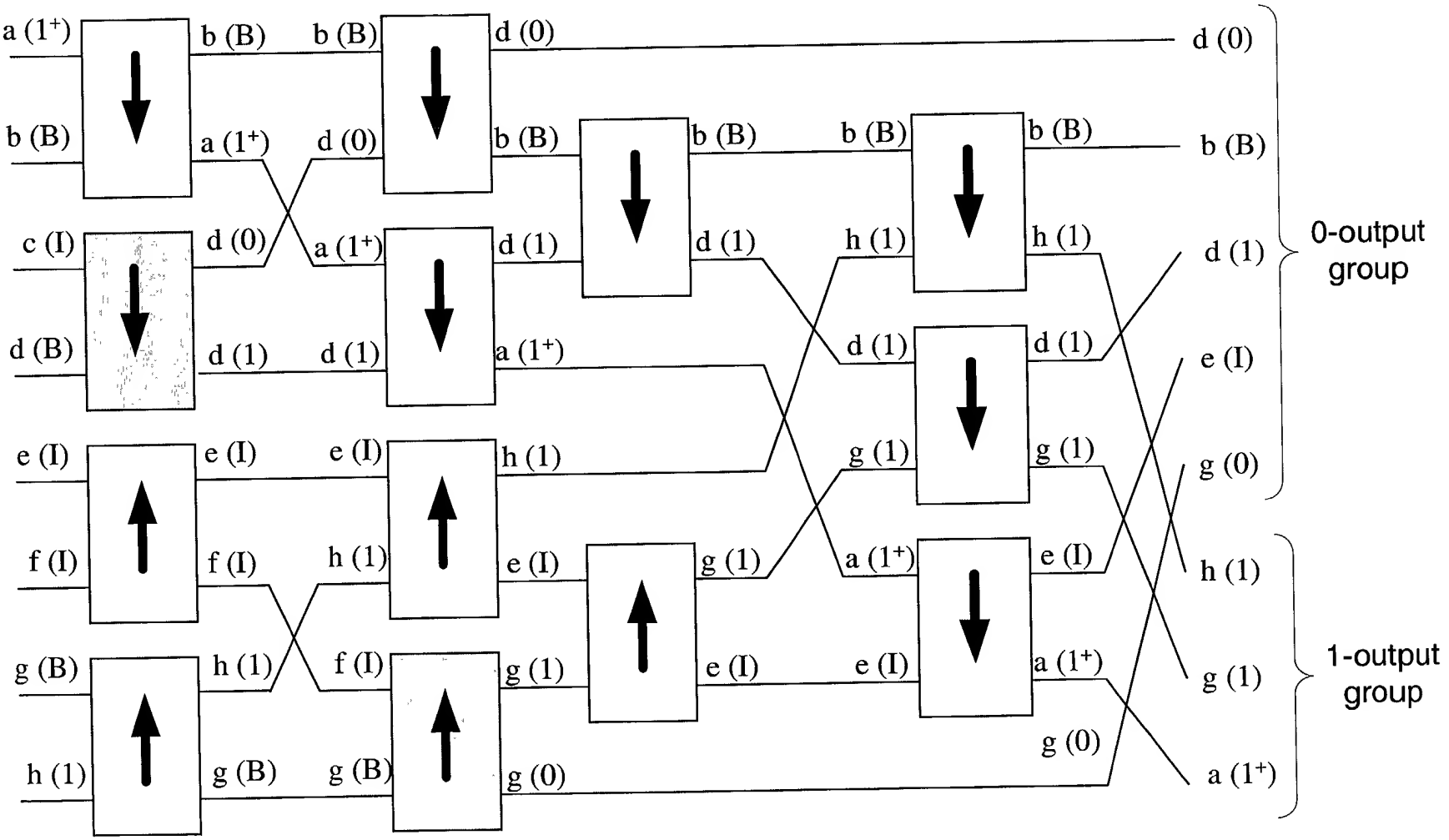

a (1+)
b (B)
c (I)
d (B)
e (I)
f (I)
g (B)
h (1)
b (B)
a (1+)
d (0)
d (1)
e (I)
f (I)
h (1)
g (B)
b (B)
d (0)
a (1+)
d (1)
e (I)
h (1)
f (I)
g (1)
g (B)
g (0)
b (B)
d (1)
a (1+)
e (I)
g (1)
h (1)
e (I)
g (1)
a (1+)
e (I)
g (0)
d (0)
b (B)
d (1)
e (I)
g (0)
h (1)
g (1)
a (1+)
0-output group
1-output group

FIG. 72A

7200

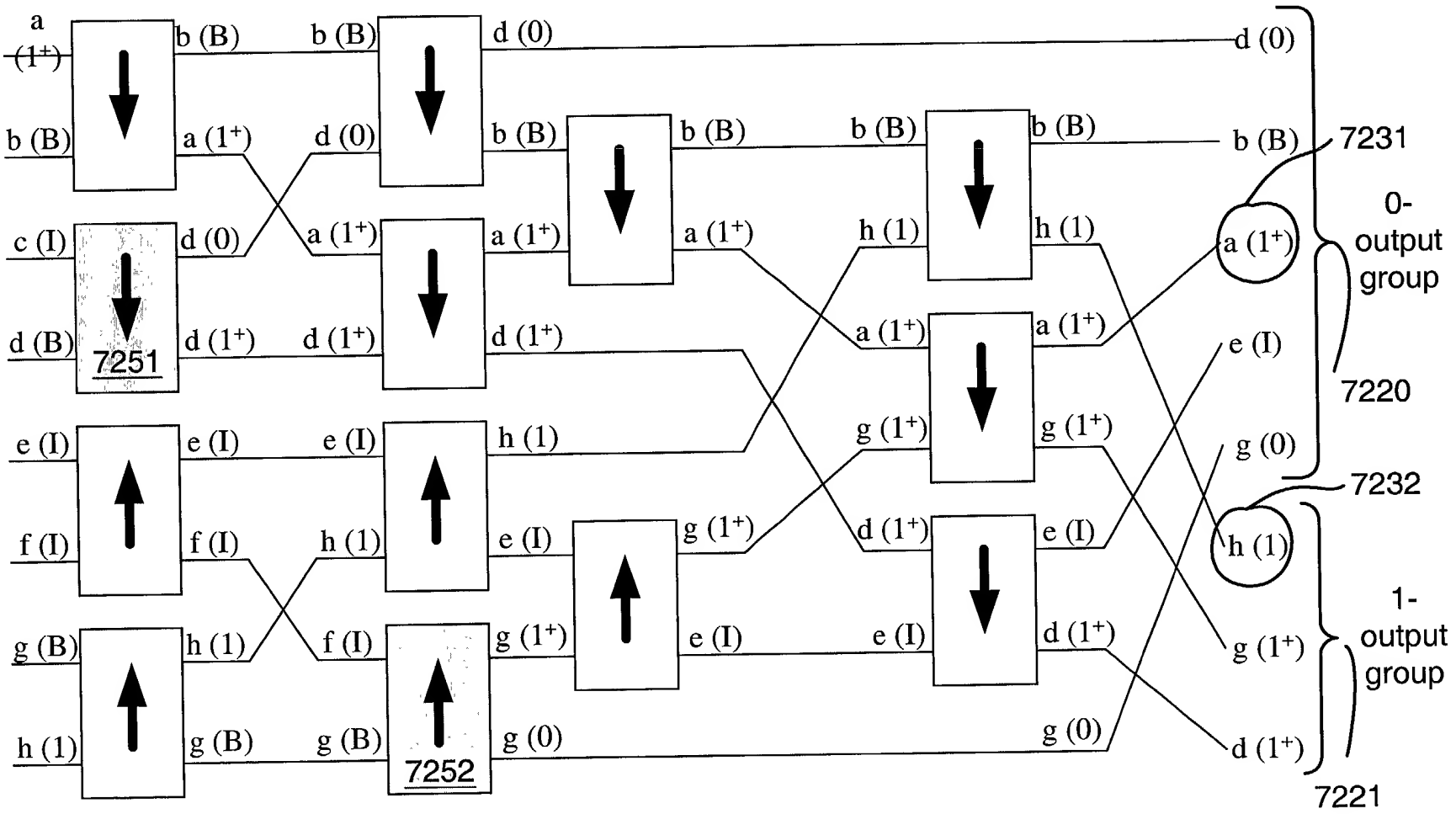

a (1+)
b (B)
c (I)
d (B)
e (I)
f (I)
g (B)
h (1)
7251
7252
7231
0-output group
7220
7232
1-output group
7221

FIG. 72B

Patent Application

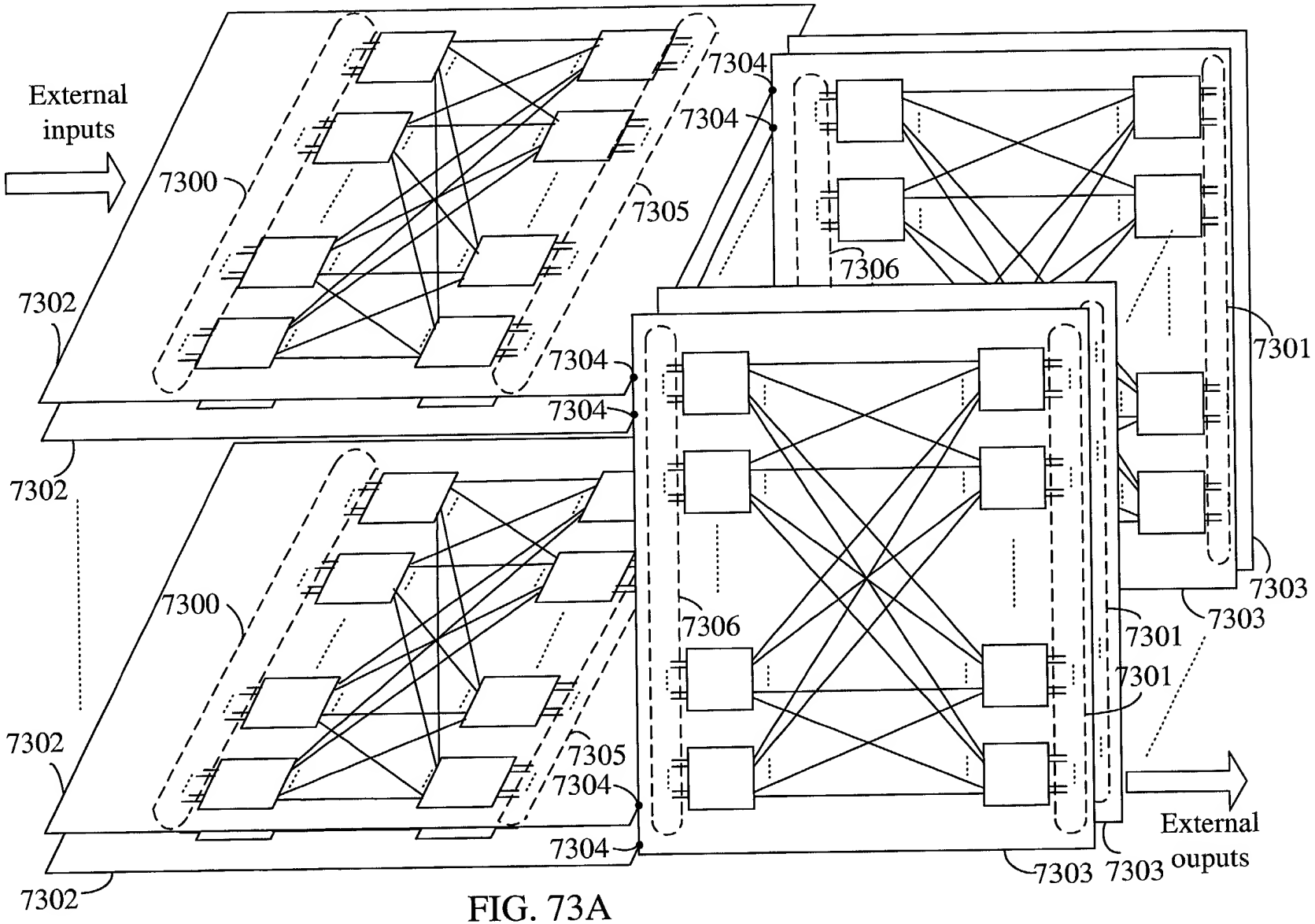
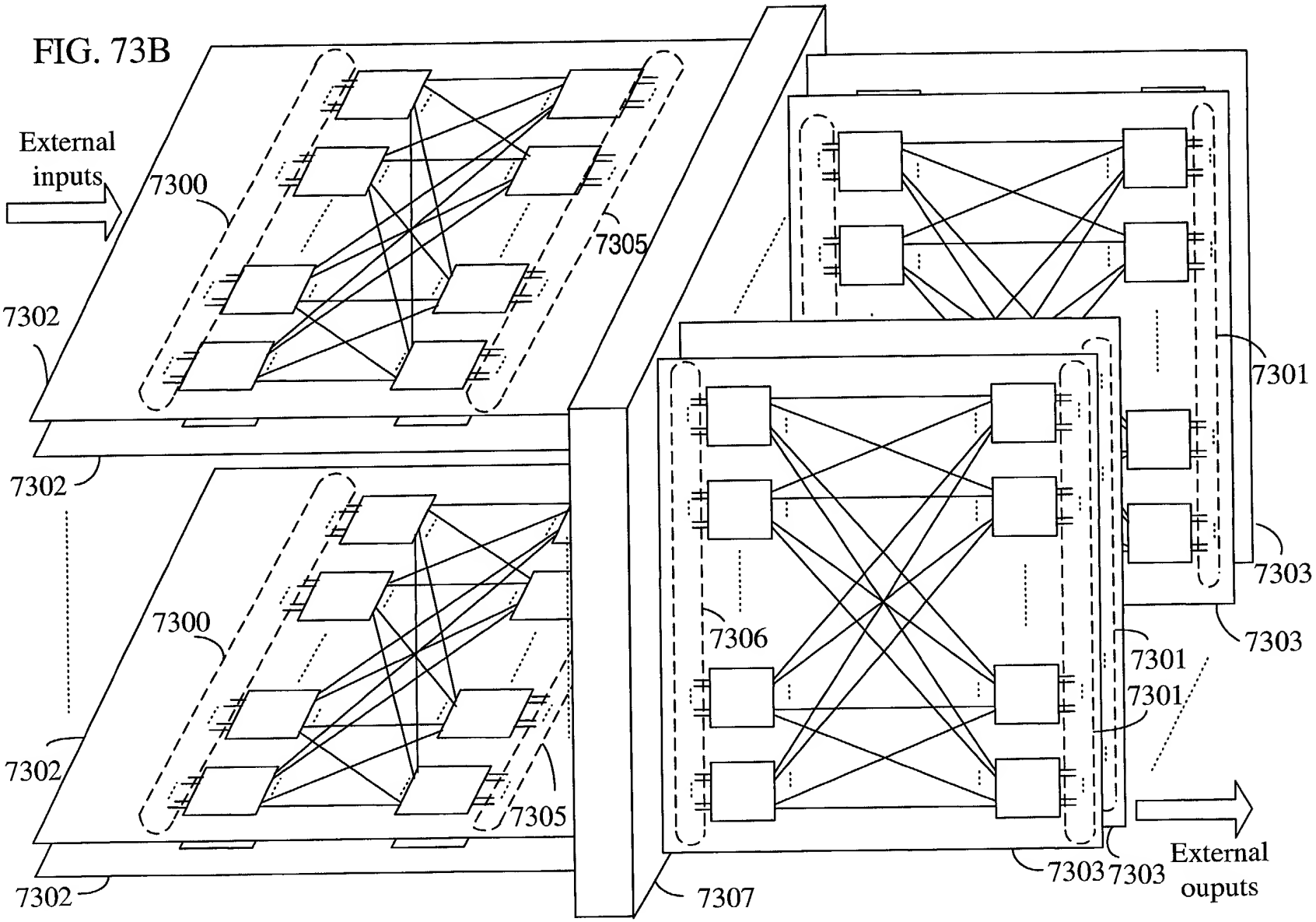



FIG. 73A

FIG. 73B


External inputs
7300
7305
7302
7302
7300
7305
7302
7307
7306
7301
7303
7303
7301
7301
7303
7303
External ouputs

PCT/US2005/028605

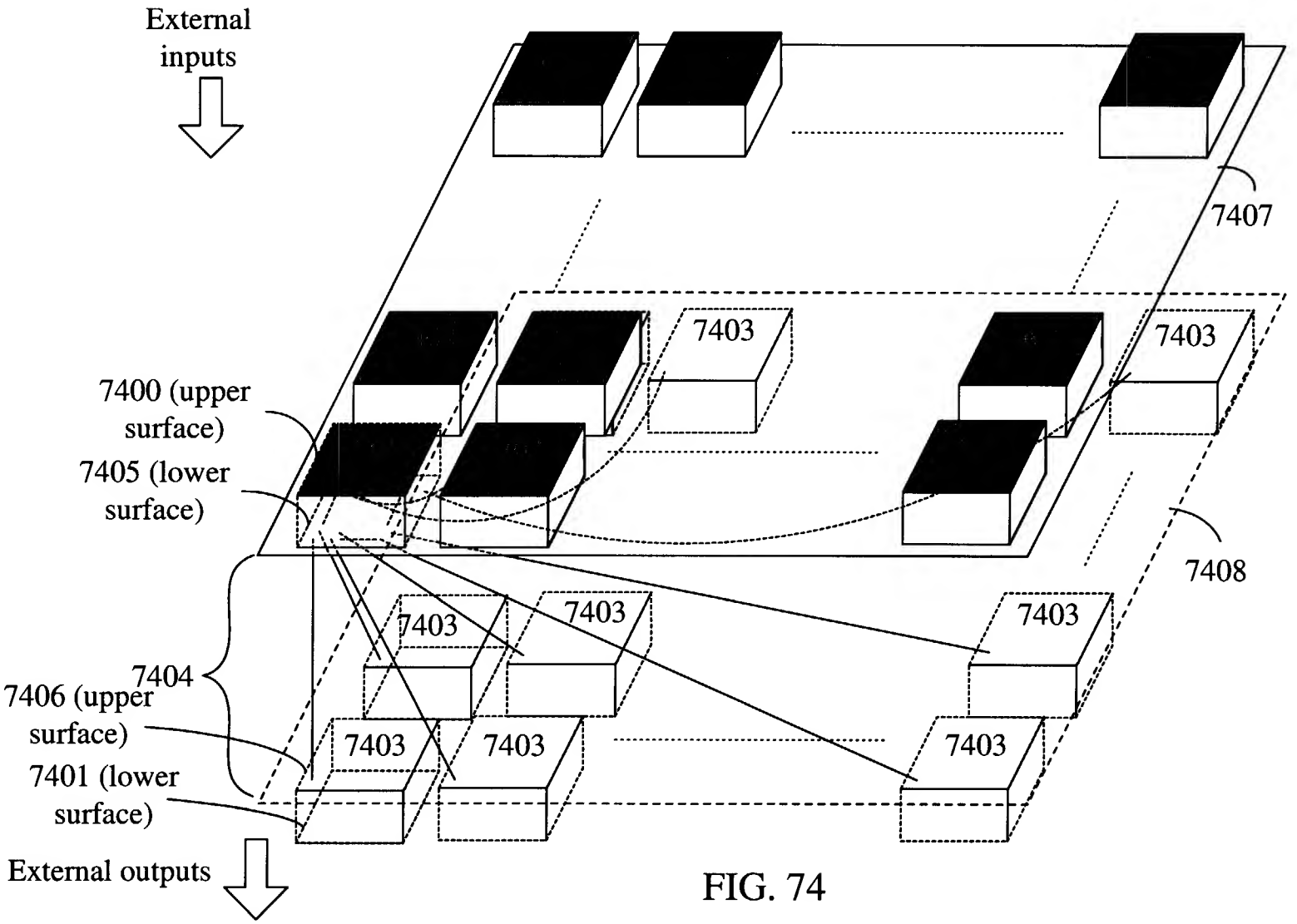
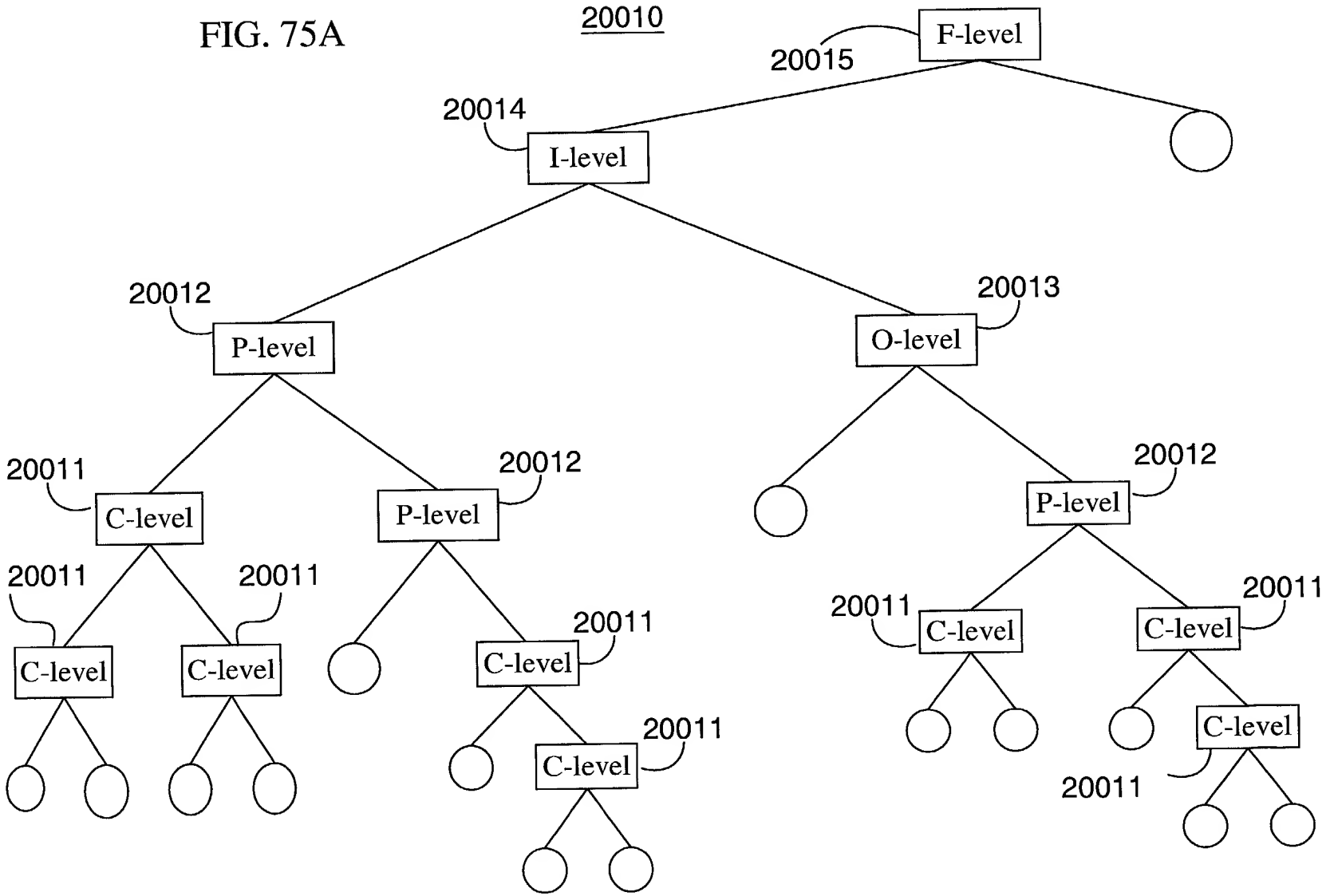



FIG. 74

FIG. 75A


20010
F-level
20015
20014
I-level
20012
P-level
20013
O-level
20011
C-level
20012
P-level
20012
P-level
20011
C-level
20011
C-level
20011
C-level
20011
C-level
20011
C-level
20011
C-level
20011
C-level
20011

Patent Application

FIG. 75B

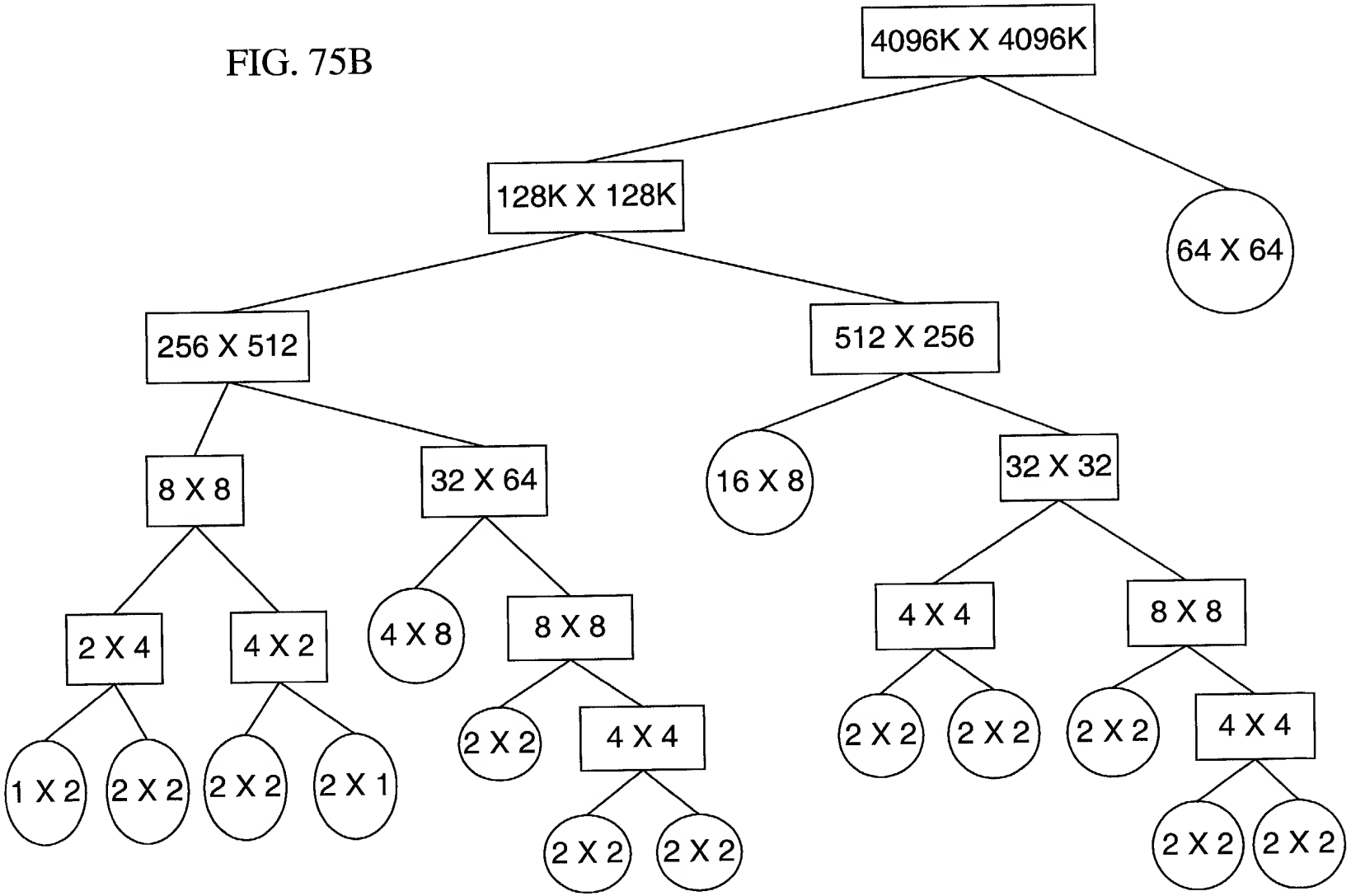
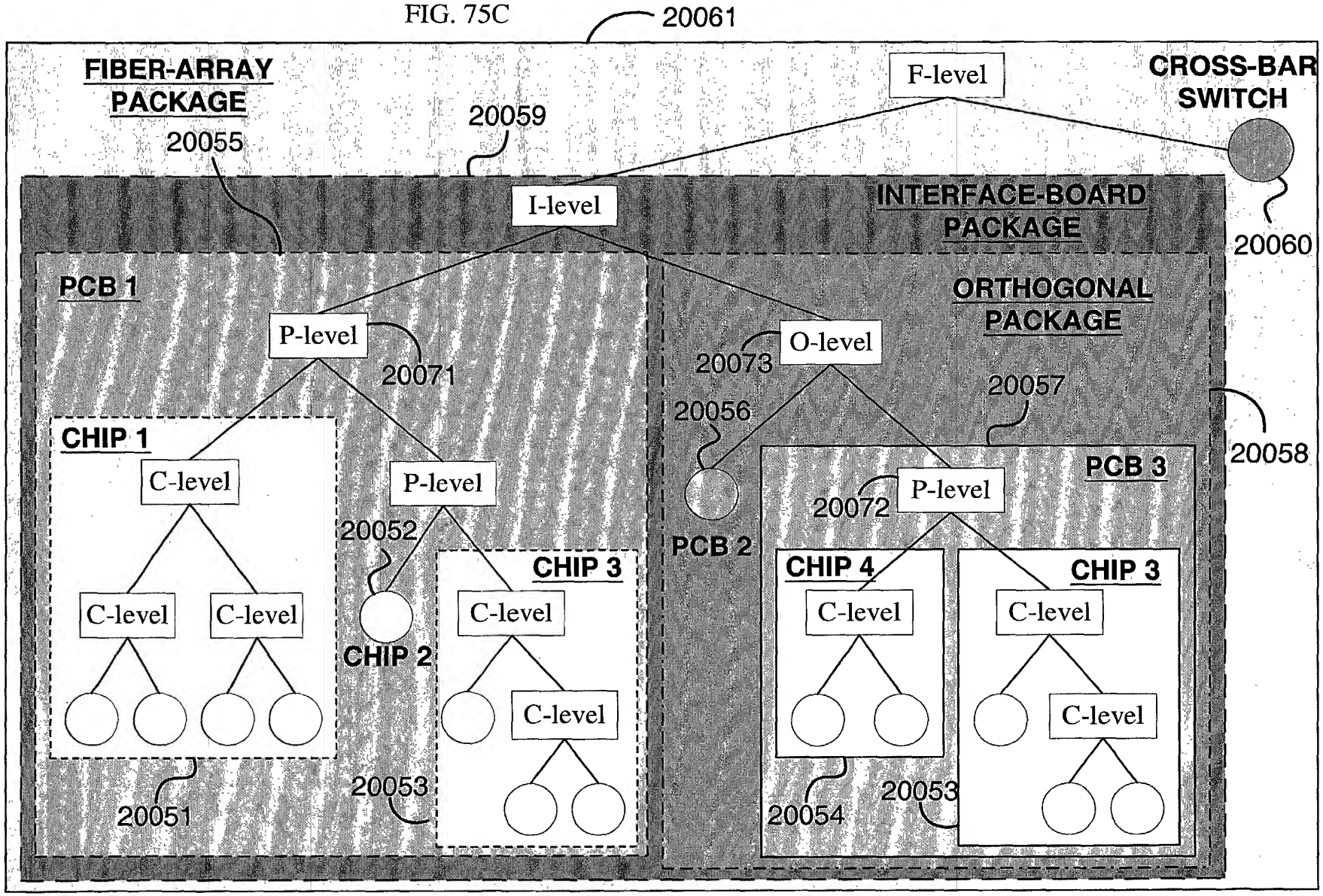


FIG. 75C


20061
FIBER-ARRAY PACKAGE
20055
20059
F-level
CROSS-BAR SWITCH
20060
I-level
INTERFACE-BOARD PACKAGE
PCB 1
ORTHOGONAL PACKAGE
P-level
20071
O-level
20073
20057
20056
20058
CHIP 1
C-level
P-level
PCB 3
20072
P-level
20052
PCB 2
CHIP 4
CHIP 3
C-level
C-level
C-level
C-level
CHIP 2
CHIP 3
C-level
C-level
C-level
20053
20051
20054
20053